



# High Efficiency, Low Cost Solar Cells Manufactured Using 'Silicon Ink' on Thin Crystalline Silicon Wafers

**October 2009 — November 2010**

Dr. Homer Antoniadis  
*Innovalight, Inc.*  
*Sunnyvale, California*

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## Scope of Work – Phase I and II

The objectives of Phase I (Feb – Oct 2009) include the development and demonstration of a 17% efficient 25mm x 25mm crystalline Silicon solar cell and a 16% efficient 125mm x 125mm crystalline Silicon solar cell, both produced by Ink-jet printing Silicon Ink on a thin crystalline Silicon wafer. To achieve these objectives, processing approaches were developed to print the Silicon Ink in a predetermined pattern to form a high efficiency selective emitter, remove the solvents in the Silicon Ink and fuse the deposited particle Silicon films. Additionally, standard solar cell manufacturing equipment with slightly modified processes were used to complete the fabrication of the Silicon Ink high efficiency solar cells.

The objectives of Phase II (Feb – Oct 2010) were the development and demonstration of a 18.5% efficient 125mm x 125mm monocrystalline Silicon cell, and a 17% efficient 125mm x 125mm multicrystalline Silicon cell, by utilizing high throughput Ink-jet and screen printing technologies. To achieve these objectives, Innovalight developed new high throughput processing tools to print and fuse both p and n type particle Silicon Inks in a predetermined pattern applied either on the front or the back of the cell. Additionally, a customized Ink-jet and screen printing systems, coupled with customized substrate handling solution, customized printing algorithms, and a customized ink drying process, in combination with a purchased turn-key line, were used to complete the high efficiency solar cells. This development work delivered a process capable of high volume producing 18.5% efficient crystalline Silicon solar cells and enabled the Innovalight to commercialize its technology by the summer of 2010.

## Phase I - Introduction

In this section we report our findings for achieving the milestones and deliverables toward completing the Phase I of our PV incubator program. As it will be shown in this report the deliverables will meet the ultimate efficiency goal of Phase I which is to demonstrate 17% efficient 125mm x 125mm crystalline Silicon (c-Si) solar cells produced by Ink-jet printing Silicon Ink on thin crystalline Silicon wafers.

*Note on deliverables:* In the original proposal, efficiency improvements were to be developed on 25mm x 25mm wafers (D3, D4 and D5) then transferred onto larger 125mm x 125mm substrates (D6, D7 and D8). However, the upgrade of the lab equipment to handle 125mm x 125mm wafers were completed ahead of schedule and as such all efficiency development has occurred on the larger substrates. In view of that we have applied the deliverables D3-D5 toward the larger substrates.

Our approach uses Silicon Ink, a Silicon nano-particle colloidal dispersion and industrial Ink-jet printing systems, to form high efficiency selective emitter on a crystalline Silicon wafer absorber. In this selective emitter device architecture the high conductivity emitter is printed by ink-jet printing an n-type doped Silicon Ink directly on a p-type crystalline Silicon wafer. This fabrication approach utilizes the same tools and materials used in a standard screen printed solar cell manufacturing line with only one additional tool, a printing system, which is used to deposit and dry the Silicon Ink in a pattern designed specifically to optimized cell efficiency. The goal of Phase I is to demonstrate a process fabrication path which has the potential to improve the efficiency of standard screen printed processed solar cells by at least 1% absolute without significantly impacting the manufacturing cost.

In this report we describe the results on **Task 1: Ink-jet Printing Development**, **Task 2: Optimization of High Efficiency Emitter Formation**, **Task 3: Cell Light Absorption Optimization** and finally **Task 4: Scale Up Process to 5" Wafers and Demonstration of 16% Cell Efficiency** all according to the description of the Scope of Work.

The milestones for Phase I are listed below:

**M1:** Demonstrate Ink-jet printing on 25mm x 25mm textured crystalline Silicon wafers with printed contact/emitter patterns having line widths of 200 microns.

**M2:** Demonstrate Ink-jet printing on 125mm x 125mm textured crystalline Silicon wafers with printed contact/emitter patterns having line widths of 200 microns.

**M3:** Demonstrate 15% efficiency on 25mm x 25mm crystalline Silicon cells incorporating optimized emitter and fused particle Silicon films.

**M4:** Demonstrate 16% efficiency on 25mm x 25mm crystalline Silicon cells incorporating optimized emitter and fused particle Silicon films.

**M5:** Demonstrate 17% efficiency on 25mm x 25mm crystalline Silicon cells incorporating optimized light absorption (optimized antireflection coatings, metallic contact grids, and front surface texturing).

**M6:** Demonstrate 15% efficient 125mm x 125mm crystalline Silicon cells incorporating optimized antireflection coating, metallic contact grid, and optimized front surface texturing.

**M7:** Demonstrate 16% efficient 125mm x 125mm crystalline Silicon cells incorporating optimized antireflection coating, metallic contact grid, and optimized front surface texturing.

**M8:** Demonstrate less than 10% degradation in the efficiency of (non-packaged) 125mm x 125mm cells after exposure to 85C/85%RH for 250 hours.

## Task 1: Ink-jet Printing Development

### Deliverables addressed in this task:

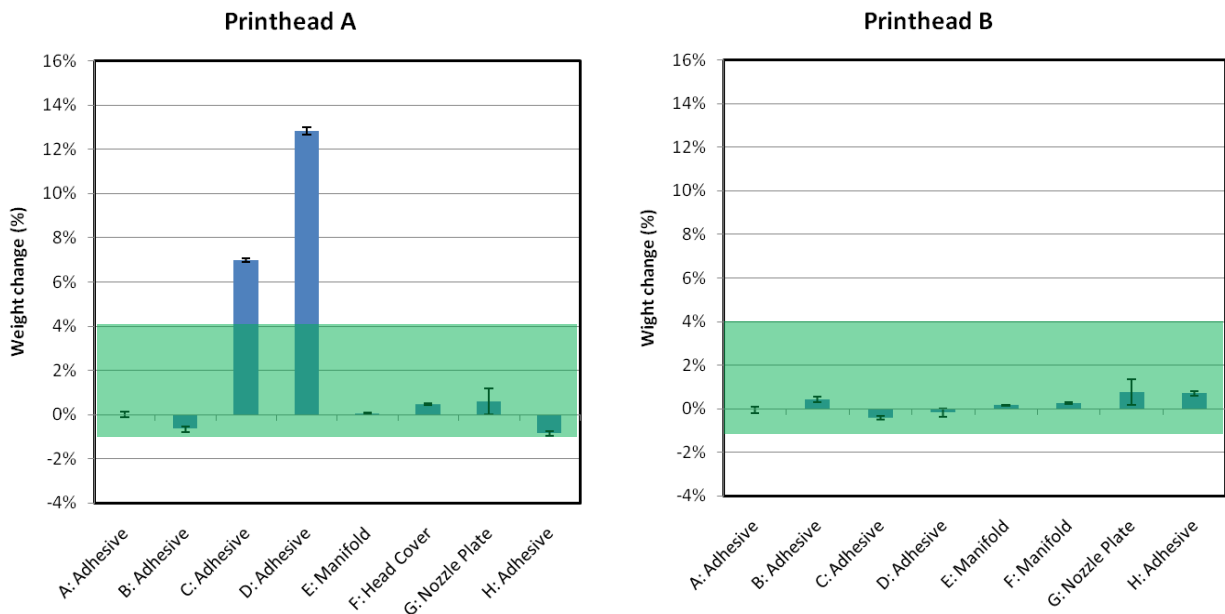
**D1:** Three 25mm x 25mm textured crystalline Silicon wafers with ink-jet printed contact/emitter patterns having line widths of 200 microns.

**D2:** Three 125mm x 125mm textured crystalline Silicon wafers with Ink-jet printed contact/emitter patterns having line widths of 200 microns.

There is a great variety of Ink-jet printhead technologies in the marketplace today. Most have been developed for graphics printing, with a select few that have been evaluated for materials deposition applications. In general, Ink-jet technology falls into one of the two main categories: thermal Ink-jet and piezo Ink-jet.

Thermal Ink-jet technology is typically used in desktop printing applications where a water based ink is partially vaporized inside the printhead. The resulting vapor bubble forms a pressure wave that ejects a droplet of ink through a hole in the nozzle plate. In comparison, in a piezo Ink-jet printhead, the pressure wave is formed by the flexing of the ink cavity wall in response to an applied voltage. Piezo technology is advantageous for Ink-jet printing of Silicon Inks because there are fewer restrictions on the ink chemistry and piezo print heads have a longer lifetime in production. Thus, we have focused exclusively on piezo Ink-jet technology for Silicon Ink deposition.

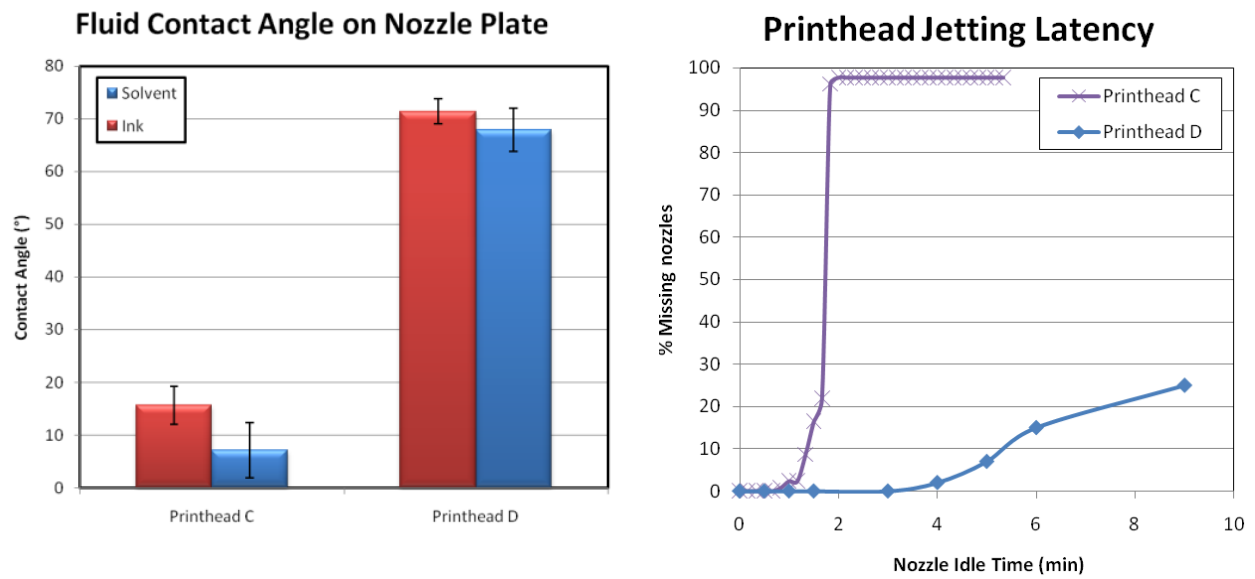
Numerous piezo Ink-jet print heads are commercially available today from companies such as FujiFilm Dimatix, Konica Minolta, Trident, Xaar, PixDro and others. Ink rheology requirements are similar for most piezo print heads, with viscosity in the range of 8-20 centipoise and surface tension 30-45dyn/cm. To avoid particle segregation and settling the ink also has to be filterable to remove all particles greater than 0.5 $\mu$ m in size. To match all of these criteria, we have had to use a set of aggressive solvents that may be detrimental to some printhead components such as adhesives and other plastics. Figure 1 shows the results of the *chemical compatibility* evaluation of Innovalight Silicon Ink when exposed to components inside two different print heads. In this case, parts of the printhead were immersed in the solvent at an elevated temperature for one week and the weight change was measured. Given the acceptable range of -1% to +4%, among these two print heads, only Printhead B is compatible with Innovalight ink. We have used similar testing and chemical compatibility guidelines to exclude several print heads from further testing.



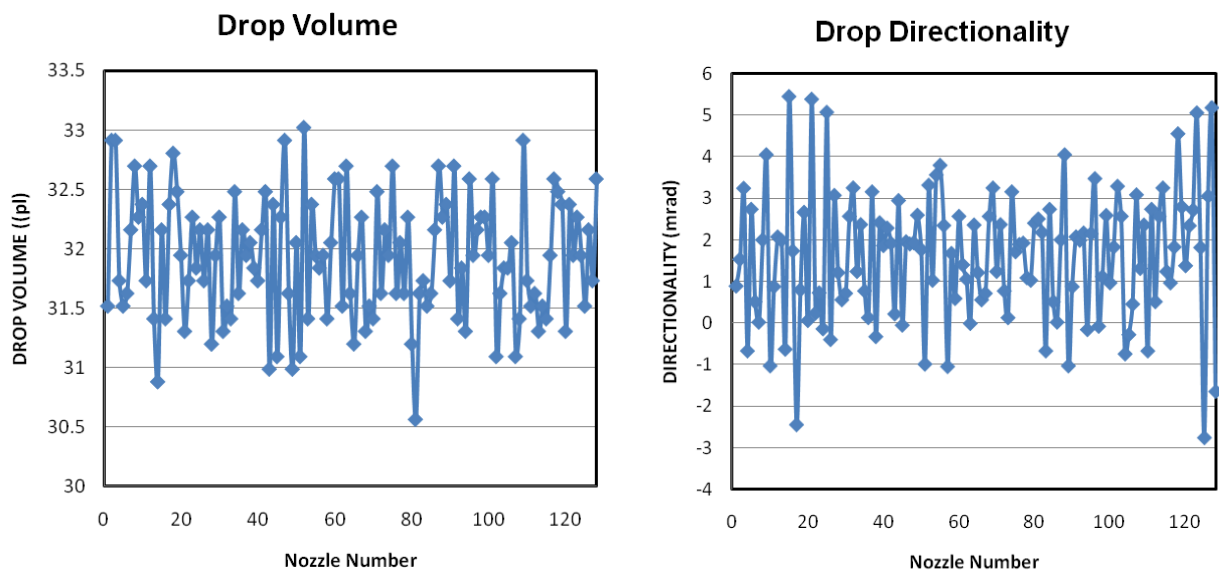
**Figure 1: Weight change of printhead components on exposure to Silicon Ink**

Another key parameter of Ink-jet printing is jetting reliability, which includes not only the ability of the printhead to jet a fluid, but also the ability of each nozzle to start jetting after an idle period, also called *jetting latency*. As the nozzle is idle, the solvent evaporates out of the ink, leaving a solid residue which can block the nozzle and cause nozzle failure. We have observed that the ability of the printhead to restart jetting after an idle time correlates with the contact angle of the jetting fluid on the printhead nozzle plate. As shown in Figure 2, the higher the contact angle of the ink on the nozzle plate, the longer the latency of the ink in the printhead. For example, the contact angle of the Innovalight ink on Printhead D nozzle plate is significantly higher than for Printhead C, resulting in increasing latency from sub 1 minute to over 4 minutes. Based on the results of the chemical compatibility testing and jetting latency, we selected printhead D for Innovalight ink printing.





**Figure 2: Contact Angle and Jetting Latency**

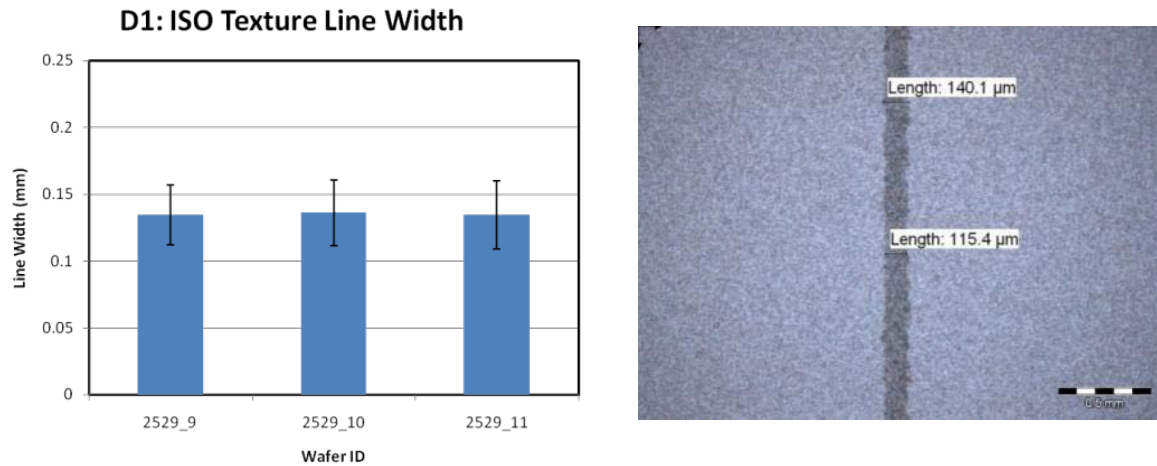


**Figure 3: Jetting Performance: Printhead D**

Figure 3 shows the jetting performance of Innovalight ink in Printhead D. The drop volume and jetting directionality are within a tight range for all nozzles allowing for deposition of fine features on Si wafers. Printhead D was selected for all subsequent printing development activities.

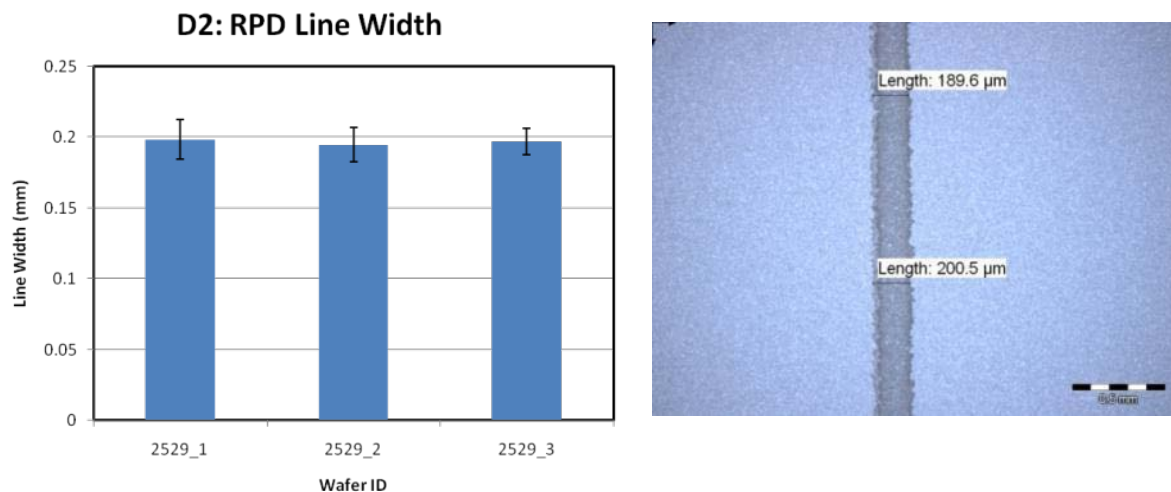
For deliverables D1 and D2, an emitter pattern was Ink-jet printed on wafers with two different surface texturization morphologies. Emitter line width results for ISO (isotropic – acidic) textured wafers are shown in Figure 4. Line width was measured using optical microscopy and an automatic pattern inspection tool on three different wafers printed using the same settings.

Substrate morphology and fluid flow cause a somewhat non-uniform line width, which varies from approximately 110  $\mu\text{m}$  to 150  $\mu\text{m}$ .



**Figure 4: Line width analysis on ISO textured wafers**

Emitter line width results for random pyramid (RPD) textured (alkaline) wafers are shown in Figure 5. Ink spreading due to fluid flow is more pronounced for this surface morphology, causing wider lines on average. For Ink-jet-printed emitter lines on three wafers, the line width ranges from 175  $\mu\text{m}$  to 205  $\mu\text{m}$ .



**Figure 5: Line width analysis on RPD textured wafers**

## Task 2 and Task 3: Optimization of High Efficiency Emitter Formation and Cell Light Absorption

### Deliverables addressed in this task:

**D3:** Five 15% efficient 25mm x 25mm crystalline Silicon cells incorporating optimized emitter and fused particle Silicon films (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

**D4:** Five 16% efficient 25mm x 25mm crystalline Silicon cells incorporating optimized emitter and fused particle Silicon films (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

**D5:** Five 15% efficient 25mm x 25mm crystalline Silicon cells incorporating optimized antireflection coating, metallic contact grid, and optimized front surface texturing (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global)

## Task 4: Scale Up Process to 5" Wafers and Demonstration of 16% Cell Efficiency

### Deliverables addressed in this task:

**D6:** Five 15% efficient 125mm x 125mm crystalline Silicon cells incorporating optimized antireflection coating, metallic contact grid, and optimized front surface texturing (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

**D7:** Five 17% efficient 125mm x 125mm crystalline Silicon cells incorporating optimized antireflection coating, metallic contact grid, and optimized front surface texturing (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

**D8:** Report reliability data demonstrating less than 10% degradation in the efficiency of (non-packaged) 125mm x 125mm cells after exposure to 85C/85%RH for 250 hours.

Innovalight has successfully developed a process for fabricating a high efficiency patterned (selective) emitter and forming electrical contacts to a solar cell using a fused particle Silicon film. Further efficiency improvements were demonstrated by optimizing the front surface texturing and antireflection coating and finally the metallic contact grid. By successfully incorporating these features onto 125mm x 125mm Silicon wafers (instead of 25mm x 25mm as originally proposed) solar cells were formed with efficiencies in excess of 17%. The processes used to fabricate these devices are all compatible with high throughput manufacturing of commercial sized substrates.

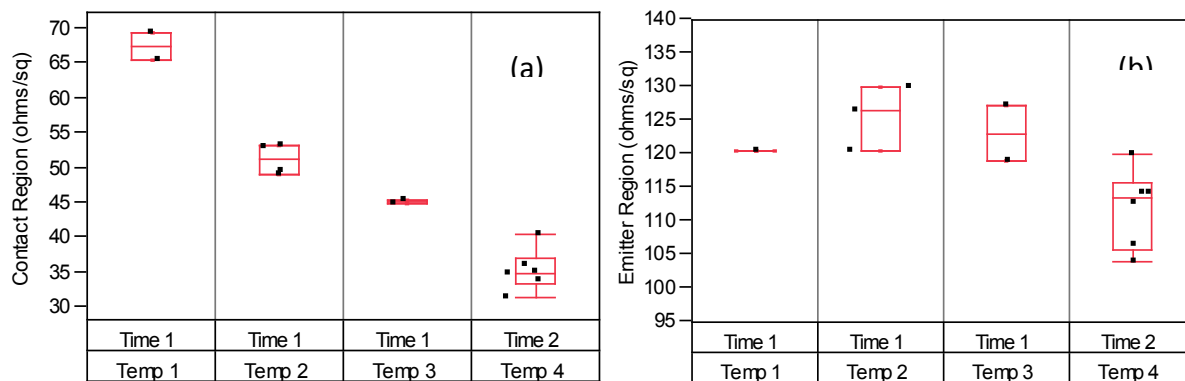
### Optimization of High Efficiency Emitter Formation:

In traditional screen-printed solar cells, a heavily doped emitter is used to both collect carriers and form ohmic contacts to a front silver electrode. The choice of the emitter doping strength requires a tradeoff between minimizing recombination (light doping preferred) and formation of a low resistance, not shunted, ohmic contact (heavy doping required). To create a high efficiency emitter it is necessary to develop a process that allows heavy doping underneath the metal contacts and light doping in the field between metal fingers. Innovalight has successfully

developed a process that uses an Ink-jet-printed Silicon Ink film to form the heavily-doped contact regions, while allowing for a uniform lightly-doped field to form between fingers.

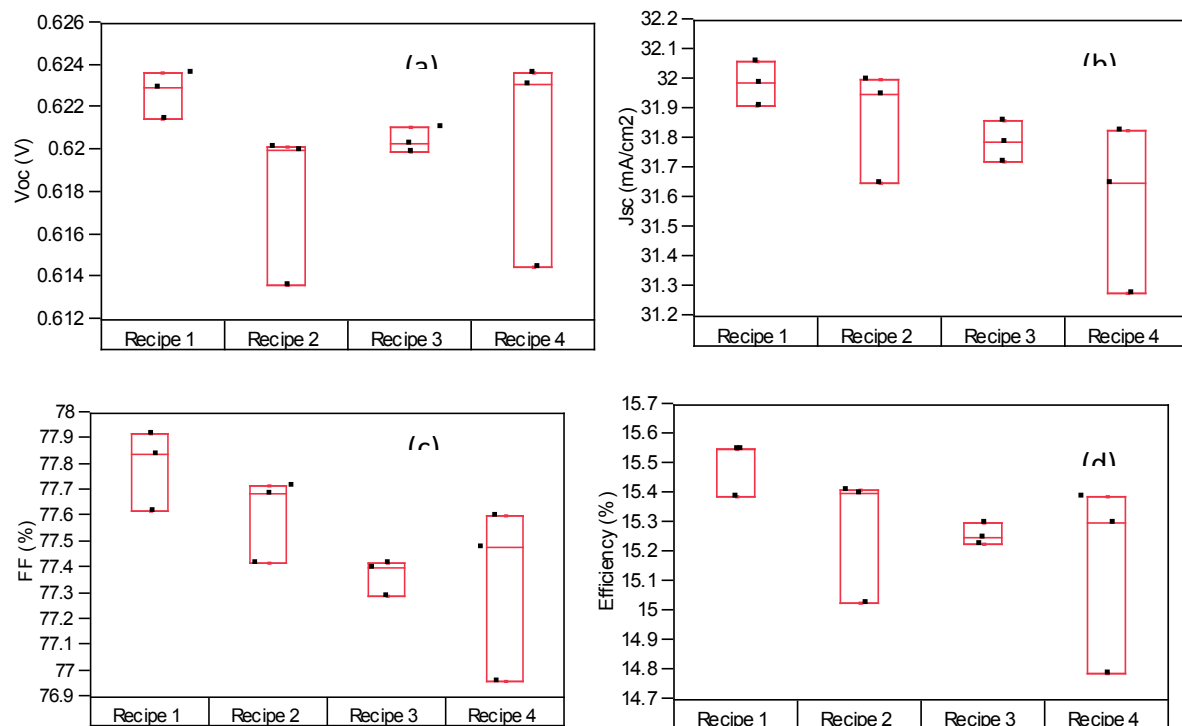
Cells are prepared on 190 $\mu$ m thick, p-type, Cz Silicon wafers. The substrates are first chemically etched to remove the layer of surface damage during wire saw. After etching, the wafers are semiconductor-level cleaned, and then an Ink-jet printer is used to deposit a layer of Silicon nanoparticle ink on the front surface. The ink is deposited in a pattern that matches the front-side silver metallization. The finger width is selected to be wider than the silver electrode to ensure good alignment in the final step. After printing, the substrates are loaded into a rapid thermal processing tool (such as an RTP or a belt furnace) and heated in an inert ambient such as nitrogen or argon to temperatures above 200°C. At these temperatures the Silicon nanoparticles start to fuse into a partly-densified film that will later be instrumental to the formation of the ohmic contact to the solar cell. The effective sheet resistance of the nanoparticle layer can be controlled by adjusting the sintering conditions.

After fusing the Silicon nanoparticle film, the wafers are loaded into a diffusion tube and an n-type emitter is formed over the surface of the wafer. This diffusion is achieved by flowing a mixture of POCl<sub>3</sub> gas to form a PSG glass layer over the surface of the wafer, then driving the phosphorous in with a subsequent temperature step in nitrogen. After diffusion the PSG layer is removed in HF chemistry, and the front surface is coated with a layer of Silicon Nitride by using a conventional remote plasma PECVD tool. The influence of Silicon nanoparticle fusing conditions (duration and temperature) on the effective sheet resistance of nanoparticle contact region and high efficiency emitter is shown in Figure 6. The thickness and refractive index of the Nitride layer are designed to minimize front surface reflection at a wavelength of 600nm.



**Figure 6: Influence of Silicon nanoparticle fusing conditions on the effective sheet resistance of (a) nanoparticle contact region and (b) high efficiency field emitter**

Front and rear electrodes are created by using a standard screen printer to deposit aluminum paste on the rear side and silver paste on the front side. The silver print is aligned such that the silver sits completely on top of the Silicon nanoparticle film. These metal pastes are baked after printing at ~200 °C and then fired to over 700 °C to densify the metal, and both to form a rear side Al BSF and to contact the silver with the nanoparticle region of the device. Device performance is dependent on the choice of firing peak temperature. The electrical results presented in Figure 7 below demonstrate how optimization of the firing recipe affects the electrical performance of Innovalight solar cells.



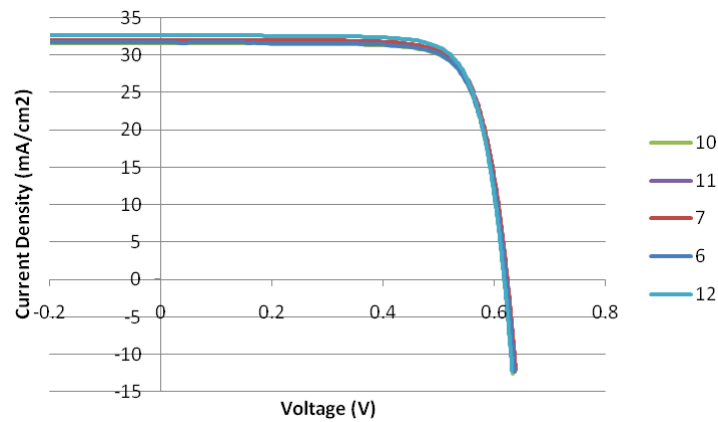
**Figure 7: Influence of different firing recipes on (a) open circuit voltage, (b) short circuit current density, (c) fill factor and (d) one-sun efficiency of Innovalight solar cells**

To finish the solar cell fabrication, a laser is used to isolate the front side emitter from the rear side contact by forming a groove.

The final device performance demonstrates that nanoparticle ink can be used to form ohmic contact to a lightly doped junction. In the cells shown below in Table 1 and Figure 8 the collecting junction used was 100-120 Ohm/sq with an equivalent doping in the nanoparticle contacts of 10-20 Ohm/sq.

Sample ID	$V_{oc}$ (V)	$J_{sc}$ (mA/cm <sup>2</sup> )	FF (%)	Efficiency (%)
6	0.621	31.67	77.22	15.19
7	0.623	32.03	77.21	15.41
10	0.619	31.54	77.91	15.20
11	0.622	31.92	77.77	15.43
12	0.617	32.62	77.73	15.65

**Table 1: 1-Sun electrical characteristics of Innovalight nanoparticle 125mm x 125mm solar cells**

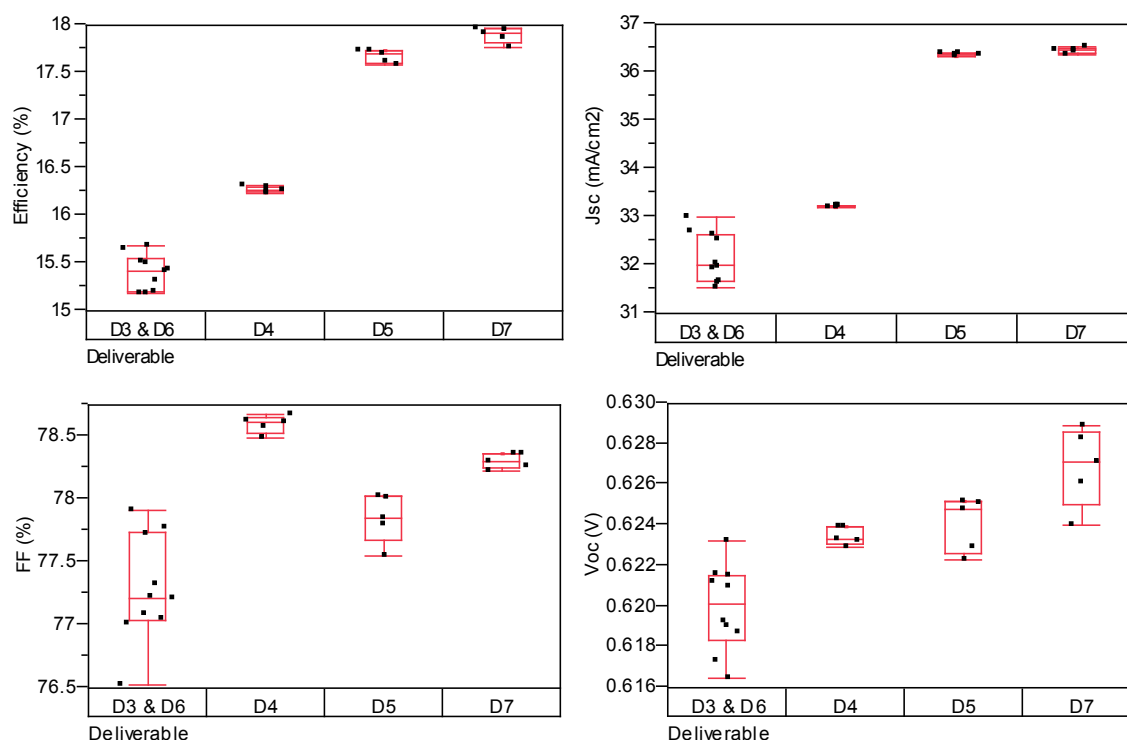


**Figure 8: One sun J-V curves for Innovalight nanoparticle solar cells**

The work presented here demonstrates that Silicon nanoparticle inks can be used to form ohmic contacts to high efficiency emitters, thus facilitating the potential for high efficiency solar cell fabrication. The fill factors in excess of 77% demonstrate the good quality of the contact formation while the open circuit voltage values over 620mV demonstrate that the ink is capable of maintaining the wafer lifetime during high temperature processing. By further optimizing the processing and incorporating other high efficiency solar cell techniques (such as random pyramid texturing) the device structure will achieve efficiencies above 18%.

### Cell Light Absorption Optimization:

Similarly with above we continued the improvement of cell fabrication process to optimize light absorption (superior light trapping) by introducing upright random pyramids on the front surface of the solar cell and by improving the optical properties of the Silicon Nitride AR coating to improve blue response. These two features were successfully combined onto 125mm x 125mm Silicon wafers to form solar cells with efficiencies in excess of 17%. A summary of the improvement in electrical performance for each deliverable is shown in Figure 9 and Figure 10 below. This was achieved by optimizing the diffusion recipe to reduce recombination and further optimization the Silicon Nitride AR coating to maximize blue response.



**Figure 9: Comparison of 1-sun electrical parameters for different deliverables.**

**Deliverable 4 (D4)**

Runsheets	Sample ID	Voc (V)	Jsc (mA/cm²)	FF (%)	Efficiency (%)	Series Resistance	Shunt Resistance
2335	10	0.6187	33.27	78.28	16.11	0.00397	169.499
2335	13	0.6196	33.23	78.34	16.13	0.00389	245.887
2335	14	0.6179	33.24	78.2	16.06	0.00401	230.44
2335	15	0.6204	33.26	78.34	16.16	0.00398	234.895
2335	17	0.6199	33.26	78.28	16.14	0.00386	214.447

**Deliverable 5 (D5)**

Runsheets	Sample ID	Voc (V)	Jsc (mA/cm²)	FF (%)	Efficiency (%)	Series Resistance	Shunt Resistance
2510	11	0.6252	36.27	77.98	17.68	0.00413	219.384
2510	14	0.6232	36.28	77.89	17.61	0.00416	91.694
2510	18	0.622	36.27	77.73	17.53	0.00433	311.224
2510	22	0.6226	36.32	77.43	17.51	0.00446	327.958
2510	24	0.6241	36.31	77.65	17.6	0.00425	277.169

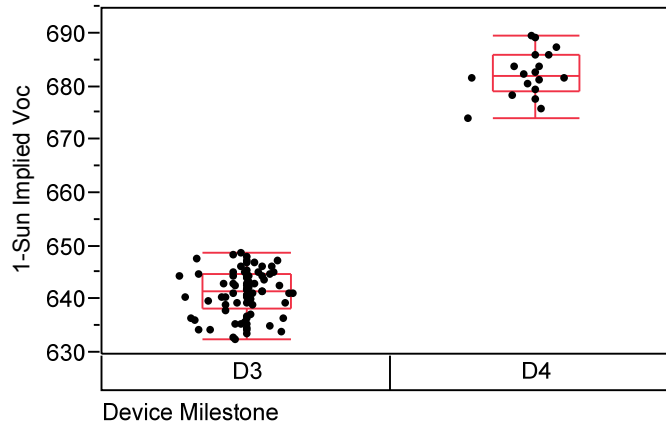
**Deliverable 7 (D7)**

Runsheets	Sample ID	Voc (V)	Jsc (mA/cm²)	FF (%)	Efficiency (%)	Series Resistance	Shunt Resistance
2514	19	0.628	36.43	78.15	17.88	0.00391	319.082
2514	22	0.6275	36.38	78.24	17.86	0.00386	282.868
2515	15	0.6245	36.36	78.11	17.74	0.00386	363.428
2515	16	0.6239	36.35	78.17	17.73	0.0039	163.735
2515	18	0.6224	36.3	78.1	17.65	0.0039	334.44

**Figure 10: Tables listing the 1-sun electrical parameters for deliverables D4, D5 and D7**

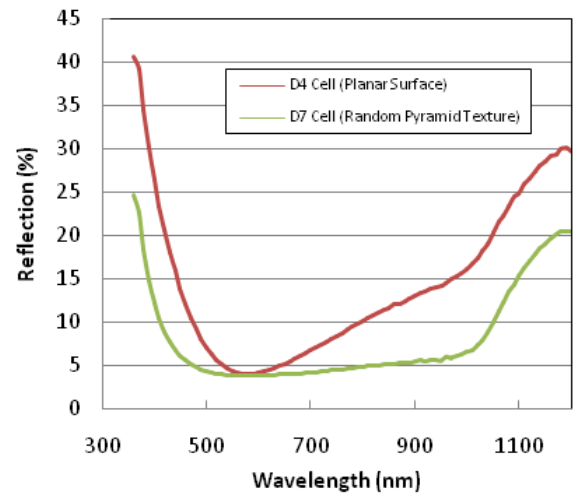
An improved diffusion recipe was developed to increase the efficiency above 16%. The diffusion recipe used to fabricate the devices in D3 and D6 was over 3 hours long and involved temperatures as high as 1000 °C. This large thermal budget resulted in increased recombination within

the device that lowered the electrical performance of finished cells. The new diffusion recipe used in D4 involves temperatures at or below 900 °C and formation of the high efficiency selective emitter in a much faster time. The reduced recombination in the substrates is evident in the One Sun Implied Voc values, shown in Figure 11, that were extracted from lifetime measurements of samples that have been diffused and Nitride coated.



**Figure 11: One-Sun Implied Voc extracted from lifetime curves for devices**

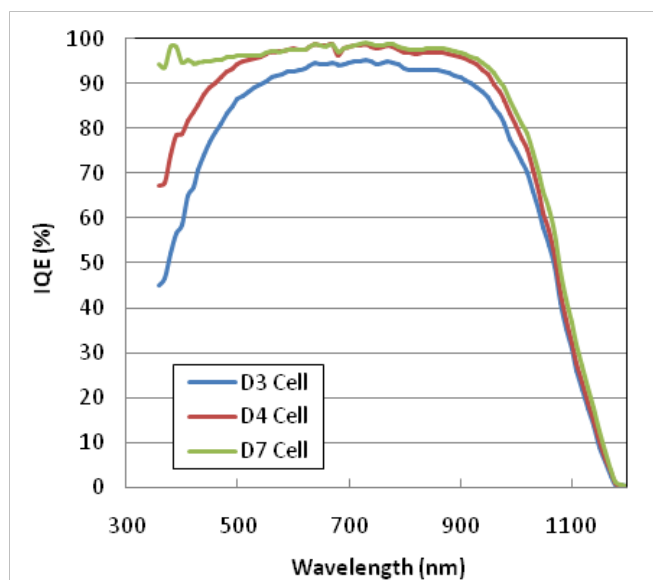
To improve the efficiency above 17% a superior light trapping scheme was integrated into the selective emitter cell process. All devices in D3 and D4 were fabricated on substrates with a planar front and rear surface. Such a surface results in a large amount of efficiency loss due to high front surface reflection. To reduce this loss, Innovalight established a standard alkaline process (based on potassium hydroxide and alcohol chemical solution) to texture the wafers with upright random pyramids. This approach is well known in the area of c-Si solar cells. It was necessary to re-optimize the ink printing, diffusion recipe, Nitride coating and screen-printing, in order to integrate this new surface morphology with the selective emitter cell. The reduction in front surface reflection of the finished cells is shown in Figure 12.



**Figure 12: Front surface reflection measured on selective emitter cells from Deliverable 4 ( $\eta=16.2\%$ ) and Deliverable 7 ( $\eta>17\%$ )**



Further gains in efficiency were realized through fine tuning of the diffusion and Nitride recipes to maximize the quantum efficiency of the cells. In particular it was necessary to optimize the Nitride properties to minimize losses due to absorption while maintaining very good passivation of the front surface. The very good blue response of cells in D7, shown in Figure 13, confirms the excellent carrier collection in the high efficiency emitter.



**Figure 13: Internal quantum efficiency measured on selective emitter cells from deliverable 3 ( $\eta=15.3\%$ ), deliverable 4 ( $\eta=16.2\%$ ) and deliverable 7 ( $\eta>17\%$ )**

### Cell Reliability:

The reliability of two batches of non-packaged 125mm x 125mm cells (5 cells each) was tested after exposing the cells in an environment of high temperature (85°C) and high humidity (85% RH) for 250 hours. We have demonstrated less than 3% degradation even after 1000 hours of exposure at 85°C/85%RH.

For this study the cells were selected from baseline runs having efficiencies above 17% (efficiency before light soak). All cells were light soaked after initial testing and sorting (to eliminate Light Induced Degradation from test results). The light soaking parameters were those typically used in the field: 30 hours under unfiltered quartz halogen lamps at One Sun at 50-60°C cell temperature (air cooled).

The cells were “batched” into 2 test groups and 1 control group. During testing they were stored in Polypropylene process cassettes. The control group was stored in a Lab cabinet. An environmental chamber by Tenny Model TJR was used for all the tests. The control was set to constant 85°C at 85% RH. The chamber operation was checked each day. Throughout the testing the position of the cells in the cassettes was rotated. For all the electrical measurements a HALM Cell Tester was used (calibrated daily according to a “silver” cell fabricated by Innovalight and referenced to Fraunhofer ISE standards).

Cells tested at convenient times throughout the workdays. They were removed from the chamber and allowed 30 minutes to equilibrate to ambient temperature before testing. Each cell

tested 3 times (contact pins were reset for each test). Average of 3 tests was taken for the “reading” for each of the electrical parameters. Data were compiled in Excel Spreadsheets.

All routine cell electrical parameters were recorded (5 parameters were selected for this program):  $I_{sc}$  (short circuit cell current),  $J_{sc}$  (short circuit current density),  $V_{oc}$  (open circuit voltage),  $\eta$  (% absolute cell efficiency), and FF (fill factor).

Little degradation was noted after the requisite 250 hours exposure. In view of that the test was extended to more than 1000 hours. Cells exposed to 85°C/85%RH Damp Heat for >1000 hours exhibited slightly different test results than the control cells, showing some effect from the exposure.

None of the tested parameters changed greater than the expected testing error (sunlight simulator testers could have an error 2% absolute for each of the tested parameters). From that we concluded that no parameter showed a significant degradation trend.

In Figure 14 below we list the measurements of the electrical parameters for two representative cells for each batch. Also in Figure 15 we show the graphs of efficiency degradation for all the cells tested in both batches.

Batch 1	0h	96h	264h	408h	600h	912h	1396h
Cell	2506-16	2506-16	2506-16	2506-16	2506-16	2506-16	2506-16
Isc	5.38	5.39	5.39	5.35	5.40	5.41	5.40
Jsc	36.21	36.29	36.30	36.03	36.37	36.40	36.34
Uoc	0.622	0.622	0.623	0.623	0.623	0.622	0.623
FF	76.93	77.10	77.13	77.13	77.17	77.08	76.95
Eta	17.32	17.41	17.43	17.31	17.49	17.45	17.42
Cell	2506-22	2506-22	2506-22	2506-22	2506-22	2506-22	2506-22
Isc	5.37	5.38	5.38	5.34	5.39	5.40	5.39
Jsc	36.15	36.23	36.24	35.95	36.29	36.32	36.26
Uoc	0.621	0.621	0.621	0.622	0.621	0.621	0.623
FF	77.15	77.13	77.03	77.03	77.07	77.02	76.99
Eta	17.31	17.36	17.35	17.22	17.38	17.38	17.38

Batch 2	0h	126h	270h	460h	772h	1252h
Cell	2508-16	2508-16	2508-16	2508-16	2508-16	2508-16
Isc	5.39	5.39	5.35	5.40	5.41	5.40
Jsc	36.29	36.31	36.01	36.35	36.42	36.36
Uoc	0.620	0.621	0.623	0.620	0.623	0.622
FF	76.95	77.03	77.15	77.09	77.25	77.16
Eta	17.31	17.38	17.31	17.38	17.54	17.45
Cell	2508-19	2508-19	2508-19	2508-19	2508-19	2508-19
Isc	5.39	5.40	5.36	5.42	5.42	5.41
Jsc	36.27	36.32	36.05	36.45	36.50	36.43
Uoc	0.620	0.622	0.624	0.622	0.624	0.622
FF	77.01	77.01	77.12	77.02	77.12	77.02
Eta	17.32	17.40	17.35	17.45	17.57	17.46

**Figure 14: Tables listing examples electrical parameter degradation under 85C/85%RH for two cells for each batch tested (Deliverables D8)**

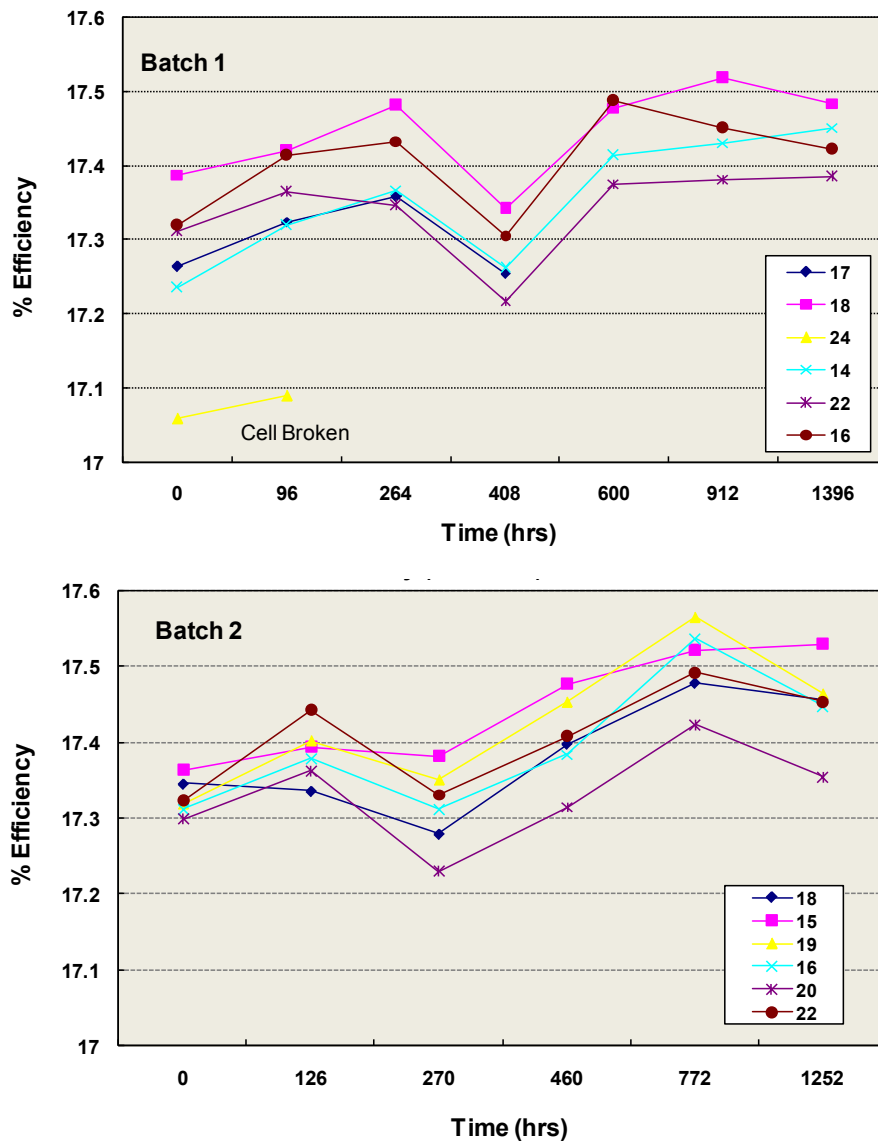


Figure 15: Cell efficiency degradation under 85C/85%RH for all cells tested for each batch (Deliverable D8)

## Stage Gate Review

During the Stage Gate Review (scheduled for Oct. 8<sup>th</sup>, 2009) the three performance metrics to be examined are:

**SG1:** 17% efficient 25mm x 25mm crystalline Silicon cells incorporating optimized antireflection coating, metallic contact grid, and optimized front surface texturing (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

**SG2:** 16% efficient 125mm x 125mm crystalline Silicon cells incorporating optimized antireflection coating, metallic contact grid, and optimized front surface texturing (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

**SG3:** Demonstrate less than 10% degradation in the efficiency of (non-packaged) 125mm x 125mm cells after exposure to 85C/85%RH for 250 hours.

## Phase II - Introduction

In this section we report our data for achieving the milestones and deliverables toward completing the Phase II section of our PV incubator program. The ultimate goal of Phase II is outlined below:

Demonstrate the use of Ink-jet and screen printing systems, coupled with ink drying processes, to complete the high efficiency solar cells in a standard cell manufacturing line.

Develop high throughput processing tools to print and fuse both p and n type particle Silicon Inks in a predetermined pattern applied either on the front or back of the cell.

Develop and demonstrate 18.5% efficient 125mm x 125mm Cz-Si cells and 17% efficient 125mm x 125mm mc-Si cells, by utilizing Silicon Ink high throughput printing technologies.

Commercialize 18.5% efficient c-Si cells by 2010.

In this report we describe the results on **Task 5: Ink-jet and Screen Printing Optimization For High Throughput Cell Production**, **Task 6: All-Back Doping and Multicrystalline Solar Cell Development** and **Task 7: Scale Up to 5" monocrystalline wafers and 18.5% Cell Efficiencies**, all according to the description of the Scope of Work.

The milestones for Phase II are listed below:

**M9:** Demonstrate operation of industrial printer patterning at the rate of at least 300 (for Ink-jet printer) and at least 1300 (screen printer) 125mm x 125mm crystalline Silicon wafers/hour

**M10:** Demonstrate increase in volume production rate to 300 wafers/hour with a 90% yield for Ink-jet patterning and to 1300 wafers/hour with a 90% yield for screen patterning of at least 1000 wafers

**M11:** Demonstrate 17% efficient 125mm x 125mm production line multicrystalline Silicon cells

**M12:** Demonstrate all back, single sided, n-type and p-type patterned doping on 125mm x 125mm monocrystalline Silicon wafers

**M13:** Demonstrate 18% efficient 125mm x 125mm production line monocrystalline Silicon cells

**M14:** Demonstrate 18.5% efficient 125mm x 125mm production line monocrystalline Silicon cells

**M15:** Demonstrate <10% degradation in the efficiency of (18% 125mm x 125mm cells non-packaged) after exposure to 85C/85%RH for 250 hours

## Task 5: Ink-jet and Screen Printing Optimization for High Throughput Cell Production

### Deliverables addressed in this task:

**D9:** Movie demonstrating operation of industrial Ink-jet and screen printer patterning at the rate of at least 300 (Ink-jet) and 1300 (screen) 125mm x 125mm crystalline Silicon wafers/hour

**D10:** Report on increase in volume production rate to 300 wafers/hour with a 90% yield for patterning with industrial Ink-jet printer and to 1300 wafers/hour with a 90% yield for patterning with industrial screen printer

### Print Platform Throughput Improvements

The focus of the second phase of the Ink-jet printing development effort was to increase overall throughput of the printing and baking tools from a peak throughput of fewer than 50 wafers/hour to over 300 wafers/hour.

### Ink-jet Printing

Initially, the Ink-jet printing was done on standalone manual printing and drying tools shown in Figure 16. The printing process was also complemented by a single wafer drying tool with a peak throughput of under 50 wafers/hour with manual loading. The goal of this work was not only to increase the throughput of the printing and drying systems, but also to automate wafer handling such that a single operator can process wafers through the integrated printing/drying system.



OTB LP50 Printer

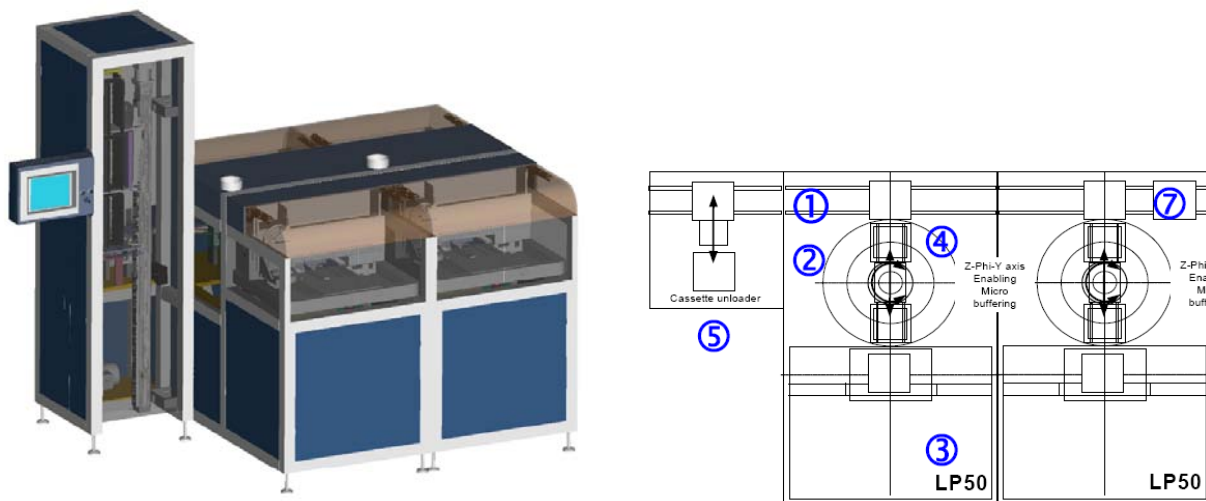


Single wafer dryer

**Figure 16: Single wafer process tools**

At the time this work was initiated, there were no tools in the marketplace meeting our requirements of high throughput, wafer handling without front side contact, printhead flexibility, integrated drying capability and chemical compatibility with the aggressive solvents used in Silicon Inks. To reduce the delivery and troubleshooting time for such a system we have focused on a tool with a modular architecture with the standalone LP50 printer as its centerpiece that retains all of its functionality. In addition to the printer the integrated system contains a handling system compatible with pilot-scale and high volume manufacturing. A 3D drawing and a schematic of the printer are shown in Figure 17. A movie demonstrating the printer/dryer tool in operation was shown as part of deliverable D-9. The Ink-jet printer was designed and manufactured by OTB Solar Engineering.

The printer system is composed of several major subcomponents. Unprocessed wafers start out in a cassette unloader **5** (cf. Figure 17 item **5**). The unloader is designed to contain up to 125 wafers at a time in 25 wafer cassettes, but can be reconfigured to a higher capacity if needed. One-by-one a robot unloads wafers from the cassettes and places them on a wafer transport belt **1** (cf. Figure 17 item **1**). The wafer transport belt carries the wafers between the unloader and several identical individual printing stations **7**. After the wafer reaches the center of the printing station the belt pauses. A dual paddle robot **4** and **2** inside the printing station picks up the unprocessed wafer from the belt and places it on the stage of the LP50 printer **3** for printing. After printing is complete, the robot places the processed wafer back on the transport belt **1** where it gets transported out of the printer units and into the dryer.



**Figure 17: 3D Drawing and Top-down Printer Schematic**

The printer architecture is designed to have maximum uptime and productivity in high volume manufacturing. One of the major challenges of Ink-jet printing in volume production is nozzle and jetting reliability. With time the quality of jetting from various nozzles degrades which impacts the quality of the printed image. To counteract the degradation in jetting performance, the printhead needs to go through a proper periodic maintenance procedure. In addition to periodic maintenance, sometimes printheads have to be taken out of service and replaced with new ones. The architecture of the printer allows for each printhead to operate and be maintained independently of the others maximizing uptime and throughput. While one printer unit is taken offline for maintenance, the others can continue processing wafers with the least possible impact on overall machine productivity. This is not feasible in other printing systems where the printheads are operated in series such that the entire machine must be taken out of service to maintain any of the installed printheads.

The belt transport system can handle wafers at a speed of 2400 wafers/hour. The overall system throughput is limited by printing throughput of individual printer modules. If additional throughput is needed, additional printer modules can be installed in line with the original modules without buying an entirely new tool to add capacity. In the configuration installed at Innovalight, each printer module can process up to 300 wafers/hour, putting the total machine throughput at 600 wafers/hour.

In order to enable high throughput processing in each printing module, we have had to implement several new features including automatic ink refill, automatic wafer alignment, and an advanced printing algorithm that allows the entire wafer to be printed in less than 12 seconds.

The ink reservoir in each printer is very small, with a volume of only 7mL. In volume production, 300 wafers/hour corresponds to ink consumption at a rate of 5-30mL/hour. Thus, to enable volume production we have implemented an automatic ink refill system, which detects the fluid level in the reservoir and refills it from a bigger ink bottle when necessary.

In the standalone LP50 printer wafer alignment is manual. This is not a viable option for wafer processing at a speed of 300 wafers/hour. We have implemented the required hardware and software modifications to enable two different algorithms of wafer alignment. First, the wafer can be aligned on the handler prior to handoff into the printer. In this method, the wafer shape is imaged while it is still on the handler. Once the wafer position on the handler is known, the position of the wafer on the printing stage can be calculated and transferred to the printer, which adjusts the print origin such that the pattern is properly placed on the wafer. The advantage of this approach is that the printer does not have to align the wafer after it is placed on the stage, enabling increased throughput. The disadvantage is that the wafer shifts somewhat during the handoff and the pattern placement error is increased. The second alignment method gives much higher pattern placement accuracy by sacrificing the throughput slightly. In this method after the wafer is placed on the printing stage the wafer edges are imaged using a fiducial camera. The wafer shape is calculated using the known edge positions and the pattern is placed appropriately.

After printing, the nanoparticle film on the wafer surface is wet. Prior to subsequent processing, the solvents need to be removed from the film without contacting the wafer surface. We have selected a belt-based warm-wall conveyor dryer to remove the solvent from the wafers without condensing on the walls of the tool.

The dryer is a customized warm-wall conveyor dryer built by MRL Industries. We have designed it such that it is fully compatible with the printer to ensure the two systems can be integrated together and the wafers can get handed off from the printer into the dryer automatically without any human input.

The complete integrated system after installation at the Innovalight facility is shown in Figure 18. A movie showing the operation of the integrated Ink-jet printer/dryer has been submitted as part of deliverable D-9.

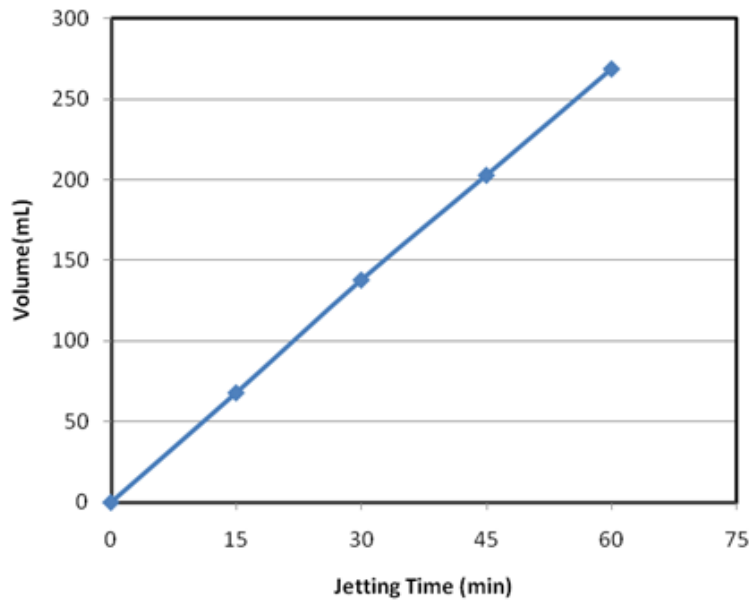




**Figure 18: Integrated Ink-jet printer/dryer after installation at Innovalight; the printer is on the left and the dryer system is on the right side**

As a non-contact printing method, the Ink-jet printing process is very gentle to the wafer minimizing wafer breakage. Over the course of a 4 hour run, we have processed over 1500 wafers with zero wafers broken, demonstrating a yield of 100%. Of the total 256 Ink-jet nozzles (two heads) present in the tool and operating in the beginning of the run, all 256 were still jetting at the end. As a result, the pattern remained unchanged throughout the run.

Furthermore the jetting reliability was demonstrated in a separate stress test of the ink/printhead compatibility. A large volume of ink was loaded into a printer and jetting was started through all 128 printhead nozzles. The volume of the jetted ink was measured as a function of time. Figure 19 shows the jetted ink volume as a function of jetting time with all nozzles firing at 10 kHz. Over the course of an hour, the jetted volume increases linearly indicating a stable jetting process with a constant drop volume. The test was stopped when there was no more ink in the reservoir. The total jetted volume exceeded 250mL which corresponds to over 25,000 wafers printed without degradation of printing performance. The two experimental tests above present an evidence and proof of our D-10 deliverable.



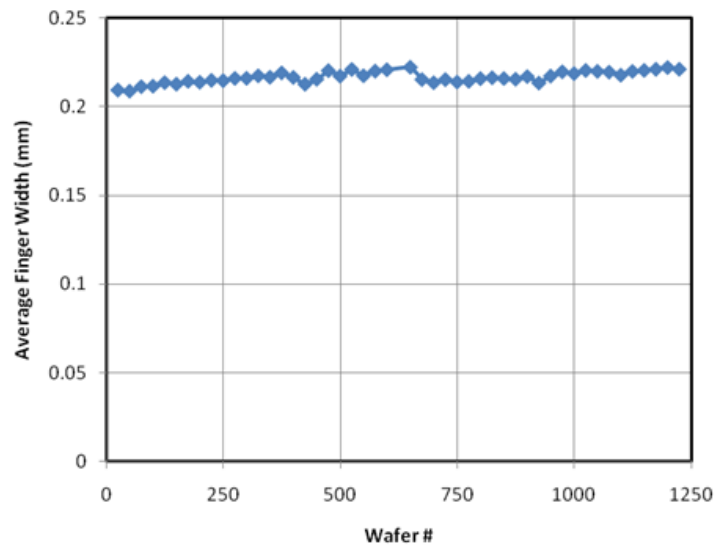
**Figure 19: Jetted ink volume as a function of jetting time with all nozzles firing at 10 kHz; jetted volume increases linearly indicating a stable jetting process with a constant drop volume**

## Screen Printing

Unlike the Ink-jet printing effort where throughput improvement required the design and fabrication of a new type of tool, equipment for high throughput screen printing of solar cells already exists. High volume screen printers for solar cell production are built by ASYS, Baccini, DEK and others. The challenge with screen printing is repeatability and stability of the printed pattern and the mechanical yield of the wafers. We have demonstrated the print performance of Innovalight Silicon Ink on a Baccini screen printer operating at 1300 wafers/hour.

Unlike the Ink-jet printing process where the digital nature of the printing process ensures the print to print repeatability of the products, in the screen printing process, multiple parameters are drifting during an extended run. From the equipment and consumables side, the screen is being repeatedly stretched and released during each print cycle, potentially impacting the shape and size of the printed pattern. Similarly, the squeegee is continuously rubbed against the surface of the screen which results in squeegee wear and impacts its shape. The rheology of the ink is also changing during an extended print run. As the ink sits on the screen surface volatile components evaporate, changing the solids content and the solvent content in the ink. Also, the repeated mechanical agitation of the ink results in repeated shear thinning of the ink which affects the constituents inside the ink and affects its viscosity.

We have optimized the Silicon Ink screen printing process and demonstrated its performance in a high throughput mode on a Baccini screen printer. A movie demonstrating the performance of the screen printer is shown as part of deliverable D-9. During the one hour run, we have printed over 1300 wafers matching the target throughput; of the 1300 wafers processed, only 3 wafers were broken, corresponding to a mechanical yield of 99.8%. This is an experimental evidence of our D-10 deliverable.



**Figure 20: Pattern fidelity of the average finger width during an extended screen printing run**

Pattern quality and fidelity on selected wafers produced during the 1300 wafer run was analyzed using an automated pattern inspection tool. As shown in Figure 20 the average finger width of the screen printed pattern does not change by more than  $15\mu\text{m}$ , demonstrating excellent pattern stability.

## Task 6: All-Back Doping and Multicrystalline Solar Cell Development

### Deliverables addressed in this task:

**D 11:** Five 17% efficient 125mm x 125mm production line multicrystalline silicon cells ( $25^\circ\text{C}$ ,  $1000\text{ W/m}^2$ , ASTM G173 global)

**D 12:** Three 125mmx125mm monocrystalline wafers doped on a single side with 12 alternating n-type and p-type doped square ( $2\text{ cm}^2$ ) pads having sheet resistance of about  $50\pm 10\text{ Ohms/sq}$  each

### 17% Efficiency Multicrystalline Silicon Solar cells

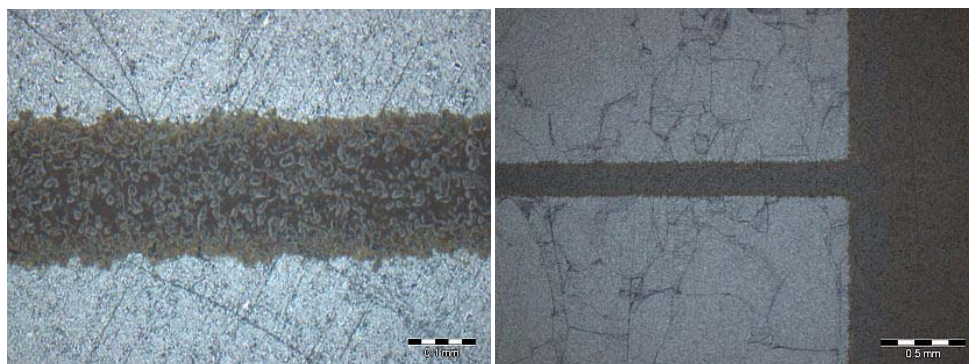
Successful application of the selective emitter cell architecture onto multicrystalline Silicon (mc-Si) has not been as widely reported as on Cz-Si wafers (we refer to this Silicon Ink selective emitter cell architecture on mc-Si wafers as “Puma Cell”). Part of the difficulty with applying high efficiency cell designs to mc-Si is the nature of the material defects and wafer quality which tend to dominate performance. High efficiency cell architectures and the processing required to fabricate them must be compatible with the mc-Si material. It has been shown that the presence of defect clusters has a strong influence on the material properties and subsequent cell performance of standard solar cells and that the efficiency gain of a high efficiency cell structure can be greatly reduced on low quality material. If the bulk quality of the material is decreased to the point that it dominates the cell performance, the advantage of reducing the surface recombination can be diminished. It has also been observed that the defected regions

in mc-Si wafers cannot be very compatible with certain high efficiency processing steps, for example high temperature furnace processes and chemical etch back.

The focus of this task was to transfer the process from Cz-Si onto mc-Si and demonstrate that the process works well on such a different type of substrate. We then examined how the material quality affects the efficiency gain provided by the mc-Si Cells reduced front surface recombination.

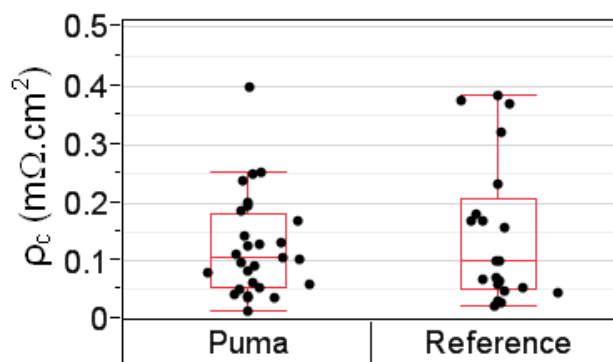
### Silicon Ink on mc-Si wafers

One of the potential obstacles in transferring a printed Silicon Ink based process from Cz-Si to mc-Si wafers is the change in wafer surface. High efficiency Cz-Si wafers tend to be textured in an alkaline solution to form random upright pyramids, a surface which is relatively uniform across the wafer. In contrast, the mc-Si wafers used in this work were textured using the acidic texturing technique which often results in very different surface features depending on the individual grains and localized defect sites. If the surface coverage of the Silicon Ink is inadequate on this surface then the device performance is expected to show an increased series resistance and a reduced open circuit voltage, similar to the effect seen for misalignment of the silver to the ink regions previously reported. Microscope images of the Silicon Ink on the surface of mc-Si wafers are shown in Figure 21 for ink after printing (left) and after low temperature baking (right). The defects on the surface were observed to cause no significant distortion in the printed ink pattern. SEM images of the Silicon Ink viewed in cross-section (not shown) also indicate good surface coverage.



**Figure 21: Optical microscope images of printed Silicon Ink on defective mc-Si surface**

Measurements of the specific contact resistivity, shown in Figure 22, verify that the Silicon Ink process worked well electrically on the acidic textured surface. The average value of  $0.1\text{m}\Omega\cdot\text{cm}^2$  is not expected to contribute significantly to the total cell series resistance. For comparison the extracted values from a  $57\text{ }\Omega/\text{sq}$  homogeneous emitter reference cell are also shown. These values are very similar to those of the more lightly doped selective emitter cell, which combined with the increased  $V_{oc}$  discussed later in the paper, verifies the effectiveness of the Silicon Ink contacts on the acidic textured surface.



**Figure 22: Specific contact resistivity (left) for Selective Emitter Cells and (right) 57 Ohm/sq homogeneous reference cells**

### Effect of Material Quality

Compared to Cz-Si wafers, mc-Si wafers tend to have overall lower bulk lifetimes and contain a percentage of defect clusters and grain boundaries which represent regions of extremely poor material quality. To improve the cell efficiency, the Puma Cells should reduce the front surface recombination while maintaining the long wavelength response of the device. This task is somewhat straightforward on Cz-Si wafers since they tend to be robust against most processing steps. However the situation is more complicated on poor quality material. For example it is necessary to achieve an appropriate amount of gettering to improve the lifetime, while avoiding high temperature steps which can degrade the material quality. It is also necessary to investigate how effective the high efficiency emitter is in regions with very high concentration of defect clusters.

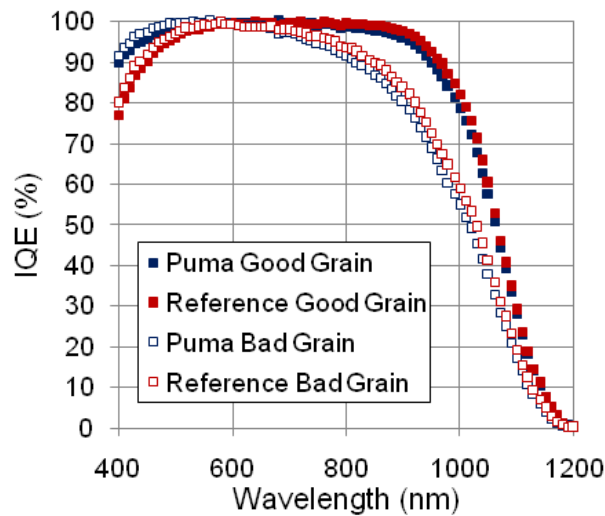
Internal Quantum Efficiency (IQE) spectral response measurements (Figures 23 and 25) and Light Beam Induced Current (LBIC) images (Figure 24) demonstrate the performance of the Puma Cells in regions of different material quality. An enhancement in the blue response is observed over the entire Puma cell, even in regions with high defect density. The blue response measured in good regions and bad regions, shown in Figure 25, also shows no significant difference due to local material quality. This observation has also been previously reported by other groups using selective emitters on mc-Si.

The slight inhomogeneity (horizontal stripes) observed in the blue response shown in the LBIC is attributed to interaction with the rollers used to position the wafers during the inline Phosphosilicate Glass (PSG) removal as well as non-uniformity in the Nitride deposition. Further optimization of these processes is expected to further improve the cell performance.

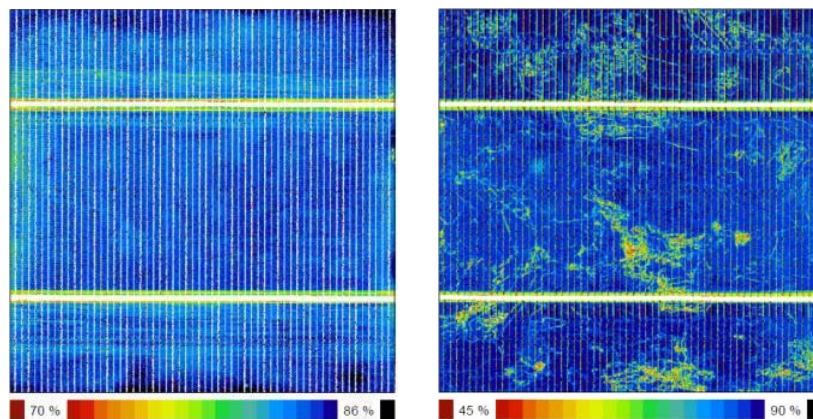
The effect of material quality on the performance of Puma cells is demonstrated further by the One Sun electrical data plotted in Figure 26 as a function of location from within a mc-Si brick. Electroluminescence (EL) images revealed that the wafers from the bottom of the brick have less defective regions than those from the top of the ingot. This observation is commonly made on mc-Si bricks and is typically explained by an increasing growth and propagation of defects as the ingot crystallizes from bottom to top. The effect of these defects on the cell performance is clearly seen with higher  $J_{sc}$ ,  $V_{oc}$  and efficiency for the better quality, less defective material.



The electrical benefits of the Puma Cells also show some dependence on the quality of the material. As the wafers become more defective the increase in open circuit voltage drops slightly from 8-9mV down to 6-7mV at the top of the brick. This slight decrease in delta is possibly caused by the increased percentage of the cell that consists of areas in which the local diode properties are dominated by low bulk lifetime rather than the surface recombination. Alternatively it might suggest that the Puma Platform requires further optimization to improve the lifetime of these poorer quality substrates to maximize performance in these parts of the brick. As predicted by the spectral response measurements, the Puma Cells show an even increase in the  $J_{sc}$  throughout the brick. At the extreme bottom of the brick, in the region known to have a high level of impurities, the performance of the Puma Cell is greatly reduced. One area for improvement in performance is in the FF of the devices. The Puma Cells show a much greater spread in FF than the reference cells with as much as 1% absolute difference for two selective emitter cells made on neighboring wafers. Reducing the recombination in bad regions as well as further diffusion optimization will be explored in future as ways to improve the Puma Cell FF.



**Figure 23: Puma Cell and reference cell internal quantum efficiency measured in regions identified using EL images as “good” grains and highly defective “bad” grains**



**Figure 24: LBIC images from a Puma Cell taken with (left) 409nm laser and (right) a 949nm laser**

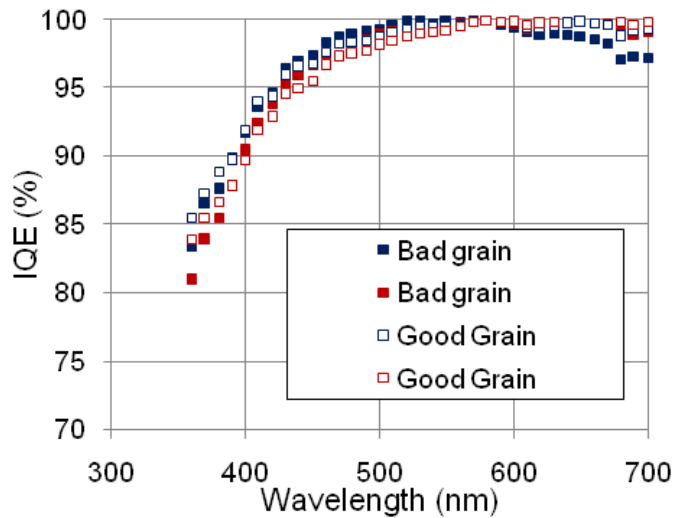


Figure 25: Puma Cell short wavelength internal quantum efficiency measured in regions identified using EL images as “good” grains and highly defective “bad” grains

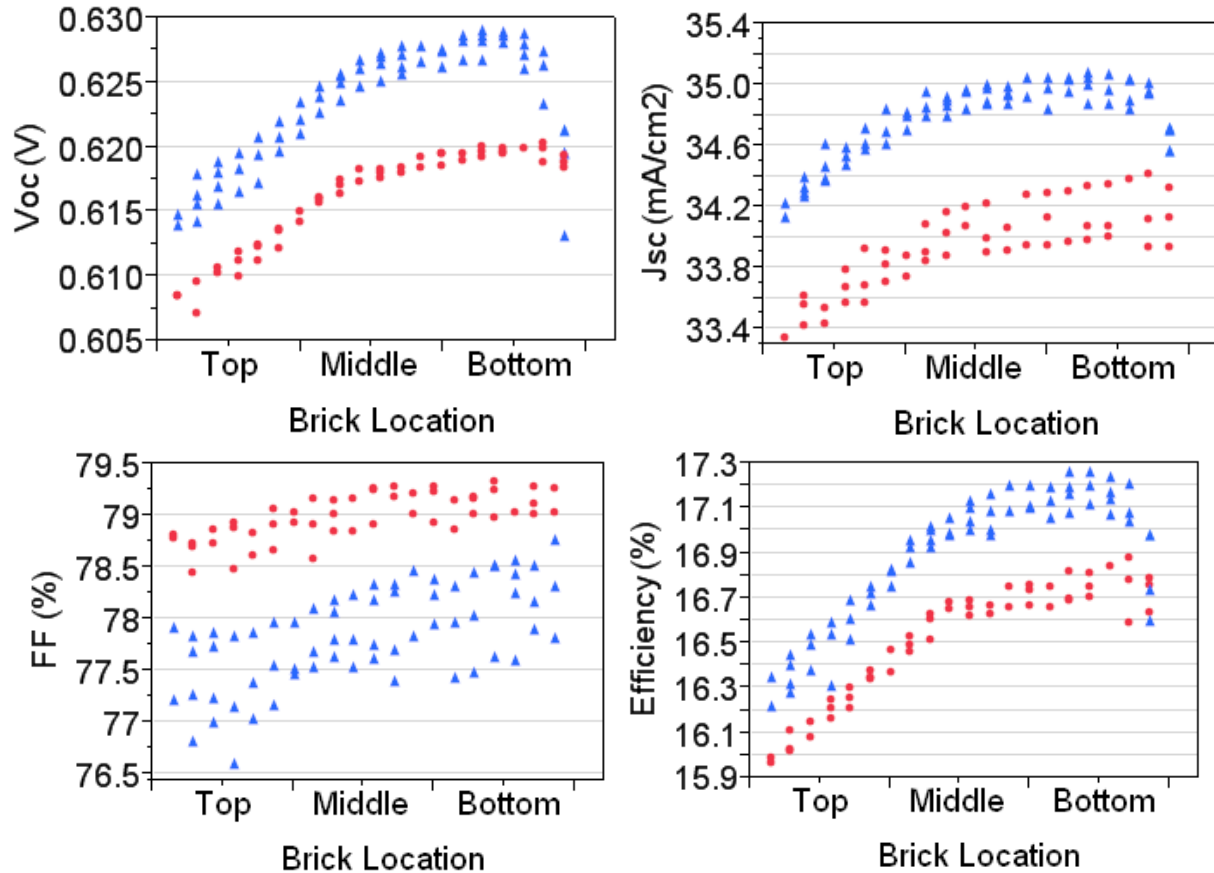


Figure 26: One-sun electrical data for several lots of Puma Cells (blue triangles) and homogeneous emitter reference cells (red circles) fabricated on mc-Si wafers as a function of location within a brick

The efficiency results for Puma Cells, summarized in Table 2, demonstrate that this technique is able to improve the efficiency of mc-Si cells across the majority of the mc-Si brick investigated.

The fact that the Puma Platform is based on the processing steps of the Cougar Platform (Selective emitter on Cz-Si wafers), which has been successfully transferred to cell manufacturers running at 1300-1500 wafers/hour processing rate, makes this a viable option for improving mc-Si cell efficiency in the industry, with potential for further improvements.

Cell Type	Voc (mV)	Jsc (mA/cm <sup>2</sup> )	FF (%)	Efficiency (%)
Puma	625	34.9	77.8	17.0
Reference	618	34.0	79.0	16.6

**Table 2: Median values for 1-Sun electrical performance shown in Figure 26**

The I-V values of the cells shipped to NREL as part of the deliverable D11 are listed in Table 3.

Cell number	Voc (mV)	Jsc (mA/cm <sup>2</sup> )	FF (%)	Efficiency (%)
5255-16	0.628	34.91	78.61	17.2
5255-14	0.628	34.93	78.57	17.2
5255-13	0.628	34.90	78.44	17.2
5253-17	0.629	34.88	78.90	17.3
5253-16	0.628	34.87	78.56	17.2

**Table 3: IV values for 1-Sun electrical performance of the Deliverable D11**

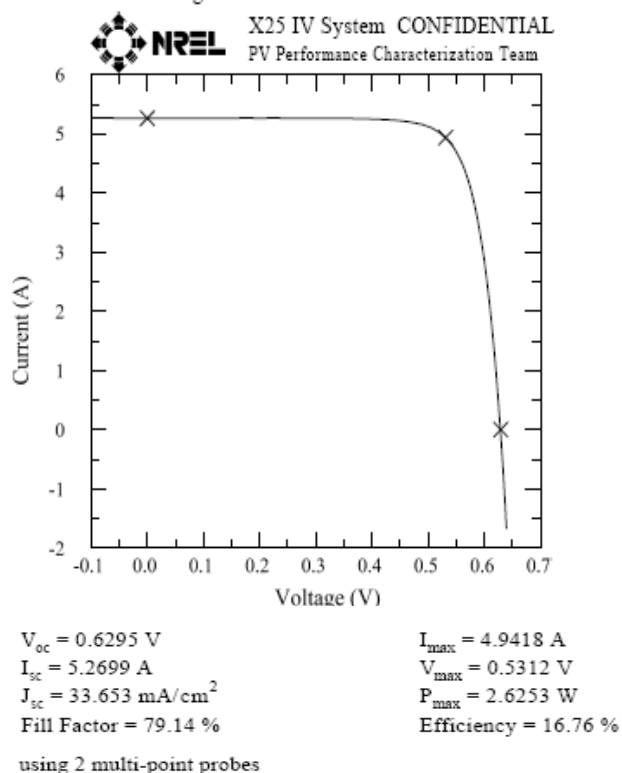
Five Puma cells processed as described above have been submitted for deliverable D11 (five 17% efficient 125mm x 125mm production line mc-Si cells (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global)

The verification of our IV measurements was performed by NREL on above five cells submitted to NREL. The IV characteristics of a representative mc-Si Puma cell are shown in Figure 27 below. The 0.4%-0.5% discrepancy between the two efficiency measurements is the result of a different probing scheme used. Innovalight is using narrow multi-probe Pogo Pings (to minimize shading) contacting the cells front and back.



## Innovalight multi-Si Cell

Device ID: 5253-17      Device Temperature:  $25.2 \pm 0.5^\circ\text{C}$   
 Jul 27, 2010 12:41      Device Area:  $156.6\text{ cm}^2$   
 Spectrum: ASTM G173 global      Irradiance:  $1000.0\text{ W/m}^2$



**Figure 27: IV characteristics for one of the mc-Si Puma cells delivered to NREL**

Future work will concentrate on further process optimization to improve the FF of the Puma Cells. By improving the FF it is expected that the efficiency delta could be improved up to 0.6% abs on high quality wafers. As wafer manufacturers continue to improve the quality of the mc-Si material and with new tools capable of binning wafers based on quality, the Puma Platform will become even more valuable for cell producers.

### All back, single sided, n-type and p-type patterned doping

For this two different screen-printable Si-ink formulations were prepared, one for n-type doping and one for p-type doping. The process to generate the two alternating series of ink squares involved two stages.

In the first stage, the p-type ink was printed on a p-type wafer as shown in Figure 28a. After a drying process, the wafers were processed through a high temperature diffusion process which generated the heavily p-type doped regions on the wafer. In the second stage of the process, the n-type ink was printed on the same wafer in a similar pattern of squares as shown in Figure 28a. After the low temperature bake to remove the solvent, the wafers were processed through a high temperature diffusion process to generate strong n-type doping under the ink.

The resulting oxide layer was removed using an HF dip and the resistivity of the printed regions was measured with an automated surface resistivity tool. Figure 28b shows the measurement locations and their measurement order.

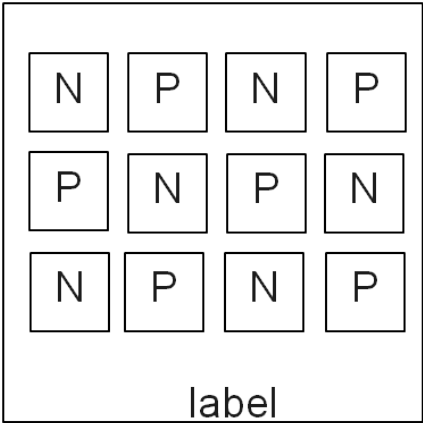


Figure 28a: Printed ink configuration

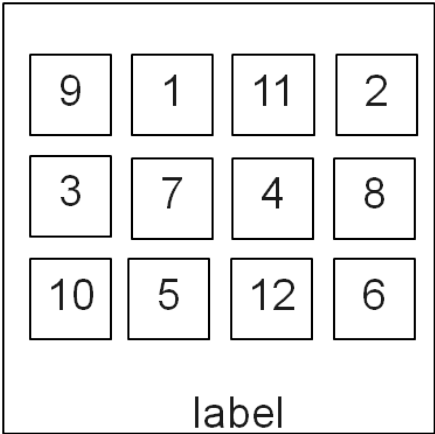


Figure 28b: Measurement locations

Figure 29 shows the average sheet resistance measured for each ink type and Figure 30 shows the measured sheet resistance as a function of measurement location. The average sheet resistance for the n-type areas is approximately 40 Ohm/sq versus a resistivity of approximately 20 Ohm/sq for the p-type squares. The sheet resistance for both inks is uniform across the wafer and is not dependent on the location of the printed pattern within the wafer. While the sheet resistance measurements of an n-type ink on a p-type wafer are numerically valid, accurate measurements of a p-type region on a p-type wafer are convoluted by the conductivity of the bulk wafer. We can calculate the resistivity of the p-doped region using a parallel resistor model for current flowing through the doped region and the bulk of the wafer. For wafer doping of 2 Ohm-cm the sheet rho of the P-type region is 24 Ohm/sq.

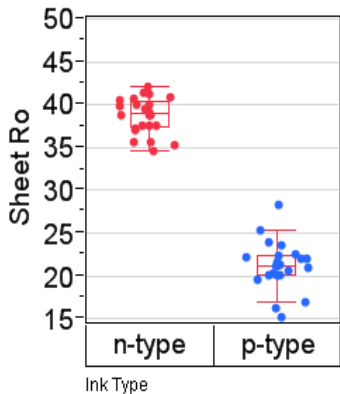


Figure 29: Measured Sheet Rho

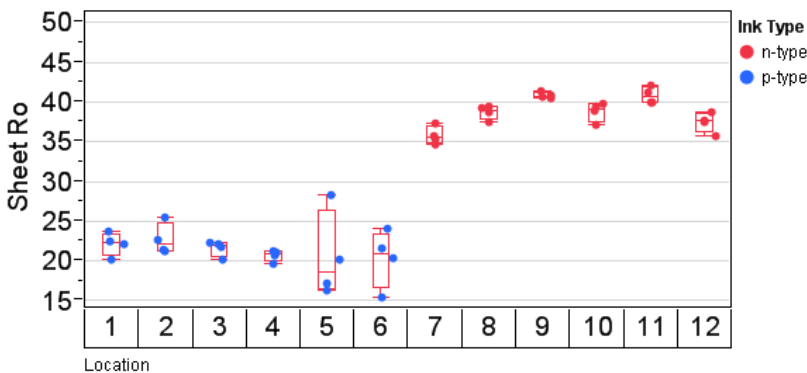


Figure 30: Measure Sheet Rho vs. Position

While the surface resistivity tool can provide useful sheet resistivity data, it cannot determine the doping type. To confirm the doping type at each location we used a hot probe method, where the voltage is measured between a room temperature probe and a heated probe. Areas with different doping type exhibit a voltage of opposite sign. Three wafers processed as de-

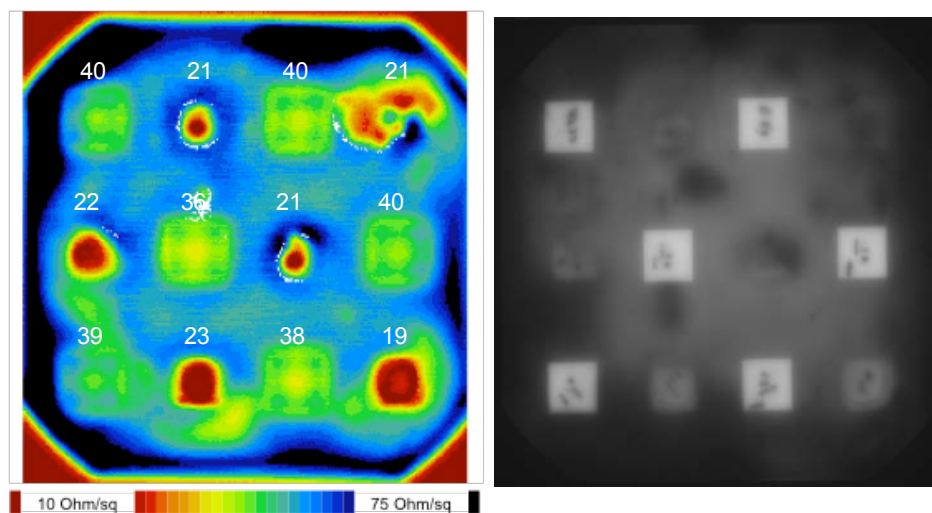
scribed above have been submitted for deliverable D12 (three 125mm x 125mm monocrystalline wafers doped on a single side with 12 alternating n-type and p-type doped square ( $2\text{ cm}^2$ ) pads having sheet resistance of about  $50\pm 10\text{ Ohms/sq}$  each).



**Figure 31: Photograph of hot probe measurements**

A typical hot probe measurement is shown in Figure 31. Heating the black probe (by using a soldering iron as depicted in Figure 31) on a p-type region results in a positive voltage measurement, whereas heating the black probe on an n-type region results in a negative voltage.

A 2D sheet resistance scan, performed at NREL, is shown in Figure 32 with the corresponding sheet resistance values indicated next to the diffused n- and p- type pads. Photoluminescence scan is also shown indicating the locations of the doped pads. Scratches of the probes are easily seen on the pads.



**Figure 32: 2D sheet resistance scan (left); Photoluminescence scan (right)**

## Task 7: Scale Up to 5" monocrystalline wafers and 18.5% Cell Efficiencies (Scale Up of Production Line Equipment)

### Deliverables addressed in this task:

**D 13:** Five 18% efficient 125mm x 125mm production line monocrystalline silicon cells (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global)

**D 14:** Five 18.5% efficient 125mm x 125mm production line monocrystalline silicon cells (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global)

**D 15:** Data in Final Report demonstrating reliability of <10% relative degradation in the efficiency of 18% 125mm x 125mm monocrystalline silicon cells (non-packaged) after exposure to 85C/85%RH for 250 hours (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global)

### 18% Efficiency Monocrystalline Silicon Solar cells

Innovalight has successfully developed a process for fabricating high efficiency patterned (selective) emitters by forming electrical contacts by using a fused nanoparticle Silicon film. The processes are all compatible with high throughput manufacturing. Solar cell efficiencies in excess of 18% have been demonstrated on commercial 125mm x 125mm monocrystalline Silicon wafers. In this report we describe the electrical results of solar cells produced in our 10MW production line.

Compared to the cells shown in the previous report, the electrical performance of these mass produced cells was improved through better metallization. Non-uniformities in the deposition thickness of the Aluminum layer were removed by improving the printing process. Broadband reflection was also reduced by incorporating slightly narrower silver line widths. Finally the FF was improved through optimization of the finger number and contact formation process. The solar cell performance (median values) is shown in Table 4 and Figure 33 below. Also the I-V characteristics of the cells shipped to NREL as part of the deliverable D13 are listed in Table 5.

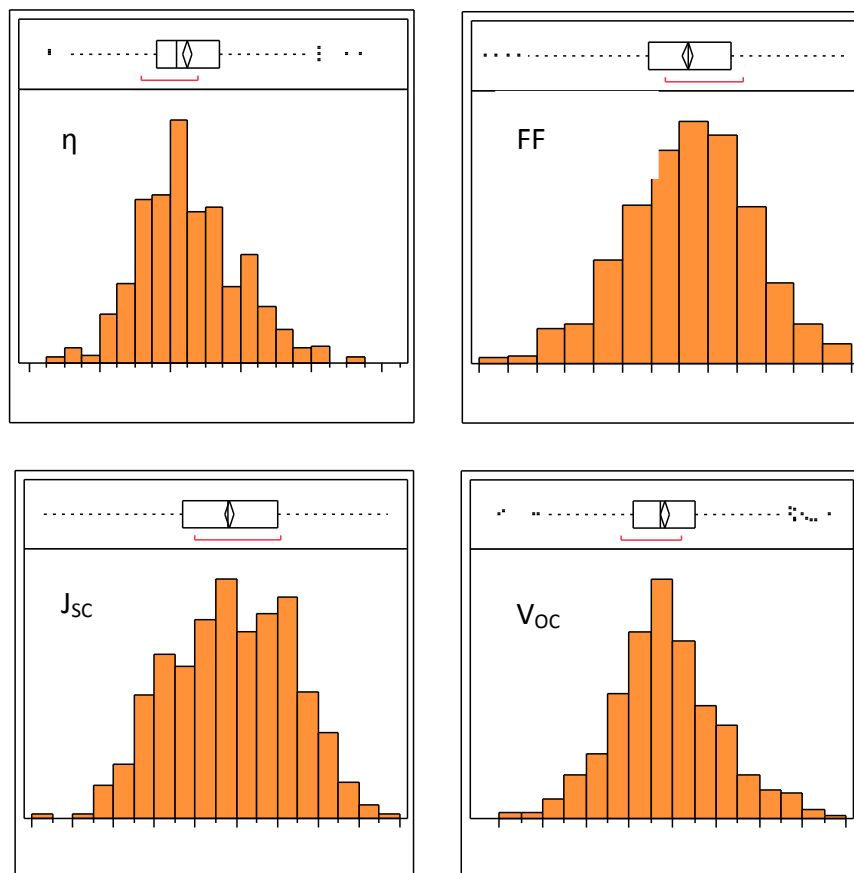
Further efficiency improvements, with median efficiencies above 18.5%, are possible through further optimization of the solar cell processing steps like improvements of metallization and Silicon Ink patterning.

Number of Cells	Voc (V)	Jsc(mA/cm <sup>2</sup> )	FF (%)	Efficiency (%)
584	627	36.88	78.8	18.2

**Table 4: Median electrical characteristics of Innovalight Silicon Ink 125mm x 125mm solar cells**

ID	Voc	Jsc	FF	Eff	Rser	Rsh
9	0.629	36.997	79.19	18.42	0.00434	434.21
10	0.628	36.983	79.16	18.40	0.00438	359.27
11	0.629	36.984	79.19	18.42	0.00436	240.72
14	0.629	37.006	79.20	18.43	0.00431	171.99
16	0.628	36.955	79.28	18.41	0.00422	513.28

**Table 5: Electrical characteristics of the 5 cells shipped to NREL as part of deliverable D13**

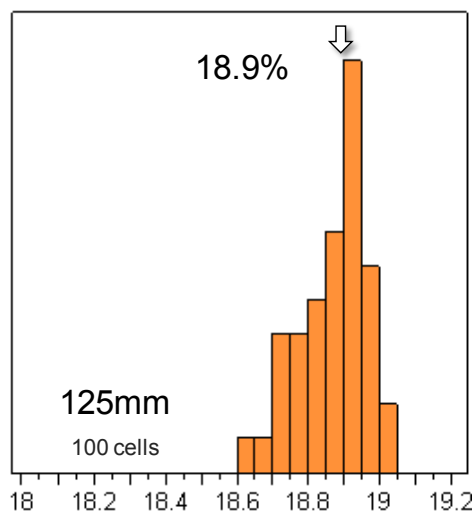


**Figure 33: Electrical characteristics of 584 Innovalight Silicon Ink 125mm x 125mm solar cells produced in the 10MW pilot production line**

Five cells processed as described above have been submitted for deliverable D13 (Five 18% efficient 125mm x 125mm production line monocrystalline Silicon cells (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

### 18.5% Efficiency Monocrystalline Silicon Solar cells

The efficiency performance of 100 cells is shown in Figure 34. Best known to Innovalight methods were used to manufacture these cells. It is clear from the graph below that the median efficiency is close to 18.9%. All measurements were calibrated against the ISE Cal Lab.



**Figure 34: Cell efficiency of 100 Innovalight Silicon Ink 125mm x 125mm solar cells produced in the Innovalight Pilot line**

Five cells processed as described above have been submitted for deliverable D14 (Five 18.5% efficient 125mm x 125mm production line monocrystalline Silicon cells (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

The verification of our IV measurements was performed by NREL on the above five cells submitted to NREL. The IV characteristics of a representative cell are shown in Figure 35 below. The 0.5% discrepancy between the two efficiency measurements is the result of a different probing scheme used. Innovalight is using narrow multi-probe Pogo Pings (to minimize shading) contacting the cells front and back.

## Innovalight mono-Si Cell

Device ID: 5167-16

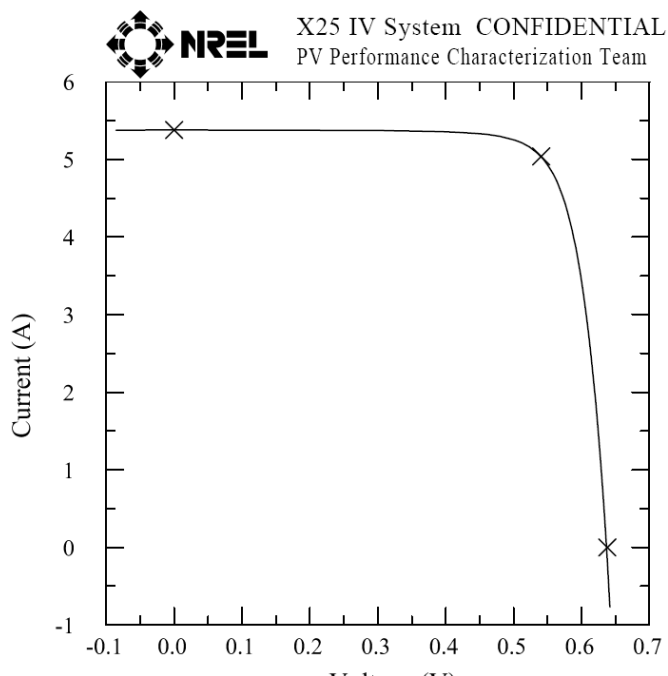
Oct 07, 2010 11:18

Spectrum: ASTM G173 global

Device Temperature:  $24.9 \pm$

Device Area:  $148.7 \text{ cm}^2$

Irradiance:  $1000.0 \text{ W/m}^2$



$V_{oc} = 0.6379 \text{ V}$

$I_{sc} = 5.3770 \text{ A}$

$J_{sc} = 36.153 \text{ mA/cm}^2$

Fill Factor = 79.37 %

$I_{max} = 5.0375 \text{ A}$

$V_{max} = 0.5404 \text{ V}$

$P_{max} = 2.7225 \text{ W}$

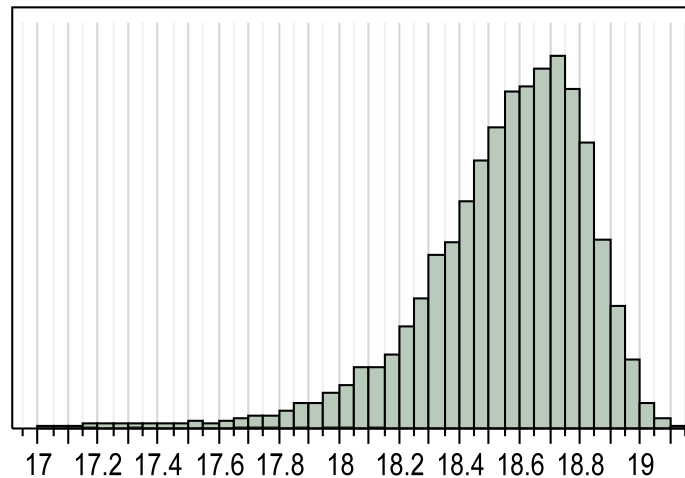
Efficiency = 18.31 %

**Figure 3 : IV characteristics for one of the c-Si cells delivered to NREL as part of the deliverable D14**

### Mass Production Cell Characteristics

Innovalight has worked closely with JA Solar, a global crystalline Silicon solar cell manufacturer and an early customer, is aggressively implementing Innovalight's process and has committed to produce at least 100 MW by the end of 2010 and more than 300 MW of cells by the end of 2011 incorporating Silicon Ink.

The statistics of the I-V data on 15,000 wafers manufactured in an automated high-throughput line are shown in Figure 36, demonstrating an average efficiency of 18.6% (compared with a baseline average of 17.6%) with max efficiency values reaching more than 19%. The mass production data demonstrates the manufacturability of the Innovalight Cougar Platform under high throughput environment and the potential of this technology to be the natural successor to the standard homogeneous emitter architecture.



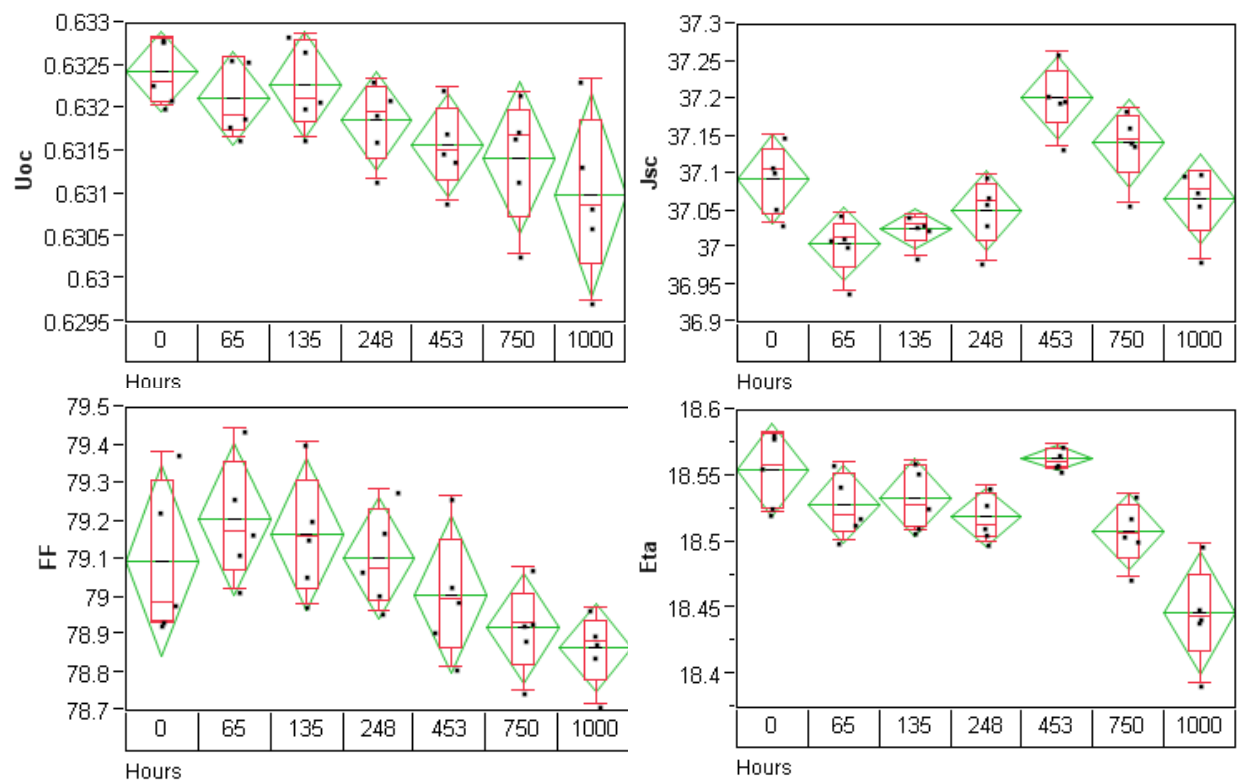
**Figure 36: Histogram of cell efficiency measured on a run of 15,000 wafers (125mm x 125mm) produced in a production facility at JA Solar**

### Reliability of 18% Solar Cells

The plots below (cf. Figure 37) represent the degradation of the IV cell parameters as a function of the time exposed under 85C/85%RH (environmental) conditions. Five complete bare (without any encapsulation) cells were used for this study. It is clearly seen in the graph below that the degradation is less than 1% thus meeting the requirements of deliverable D15 (Data in Final Report demonstrating reliability of <10% relative degradation in the efficiency of 18% 125mm x 125mm monocrystalline Silicon cells (non-packaged) after exposure to 85C/85%RH for 250 hours (25 °C, 1000 W/m<sup>2</sup>, ASTM G173 global).

Initial module reliability tests made by using the Innovalight Selective Emitter cells show similar behavior with conventional modules made with standard Cz-Si cells, thus guaranteeing, as expected, the very long term stability of this product.





**Figure 37: Degradation in cell electrical characteristics as a function of time after exposure to 85°C/85%RH environment; less than 1% degradation is observed**

## Final Review Performance Metrics

The final review of this project was successfully completed based on the metrics listed below:

1. Patterning with industrial ink-jet and screen printer at the rate of at least 300 and 1300 125mm x 125mm crystalline silicon wafers per hour respectively where 90% of the cells produced are printing defects free
2. Three 125mm x 125mm monocrystalline wafers doped on a single side with 12 alternating n-type and p-type doped square ( $2\text{ cm}^2$ ) pads having sheet resistance of about  $50 \pm 10\text{ Ohms/sq}$  each
3. 17% efficient 125mm x 125mm production line multicrystalline silicon cells ( $25\text{ }^\circ\text{C}$ ,  $1000\text{ W/m}^2$ , ASTM G173 global)
4. 18.5% efficient 125mm x 125mm production line monocrystalline silicon cells ( $25\text{ }^\circ\text{C}$ ,  $1000\text{ W/m}^2$ , ASTM G173 global)
5. Reliability of <10% relative degradation in the efficiency of 18% 125mmx125mm monocrystalline silicon cells

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